Characterisation of a Dual Frequency Conversion Superheterodyne Receiver

Wai-Man Monica Wu

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for the degree of Master of Science in Engineering.

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Declaration

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

Signature of Author .....

Cape Town

18 Feburary 2008

Abstract

The Square Kilometre Array (SKA) is an international effort to build an advanced and highly sensitive radio telescope. The South African Karoo Array Telescope (KAT) project is initiated to show the international committee of SKA that South Africa has sufficient technological background and resources to make a contribution to them. Therefore this research investigates and evaluates the performance of the Australian built 3x4 receiver module and then to verify that this prototype is suitable to be integrated into the 24-channel RF rack for KAT.

This dissertation starts off with a brief introduction of the SKA project, and explain how it relates to the KAT project. Then certain receiver design techniques and parameters will be discussed together with receiver design trade-offs will be presented. This dissertation will then focus on the actual simulations of the 3x4 receiver module using the time-domain RF simulator, SystemView. An overview of the design for the 24-channel RF rack integrated locally by Tellumat (Pty) Ltd is presented and acceptance tests will be conducted and the test results will be presented. Results obtained from both simulations and measurements are analysed and compared.

This dissertation is concluded by discussing the conclusions and recommendations are presented for how to improve the accuracy when simulating the 3x4 receiver module.

Acknowledgements

I would like to thank my supervisor, Professor Mike Inggs, for his guidance and continuous motivation assisting me to complete this dissertation. I would also like to thank South Africa SKA for financially supporting me through my study. I would like to thank Dr. Richard Lord for keeping me on track by having weekly meetings with me, and his wife, Regine Lord, for proof-reading this dissertation. Special thanks to Mario Aldera from Tellumat (Pty) Ltd for allowing me to be involved with the RF rack integration.

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Last but not least, thanks to my family, for their support and love.

Contents

List of Figures

List of Tables

List of Symbols

B	—	Bandwidth
DR	—	Dynamic Range
$f_{sampling}$	—	Sampling frequency
f_{LO}	—	Local oscillator frequency
f_{RF}	—	RF frequency
f_{IF}	—	Intermediate frequency
f_{IM}	—	Image frequency
F_n	—	Noise figure of the n^{th}component
G_{rx}	—	Receiver gain
G_n	—	Gain of the n^{th}component
IIP3	—	Third-order intercept point measured at the input
k	—	Boltzmann's constant
MDS	—	Minimum detectable signal
N_i	—	Input noise power level
N_o	—	Output noise power level
OIP3	—	Third-order intercept point measured at the output
$P1dB_{in}$	—	1 dB compression point measured at the input
SFDR	—	Spurious free dynamic range
Si	—	Input signal to the system
SNRo	—	Output signal-to-noise ratio
SNRi	—	Input signal-to-noise ratio
SINAD	—	Distortion-to-noise and distortion ratio
Ta	—	Equivalent antenna temperature
Te	—	Equivalent noise temperature
To	—	Ambient temperature

Nomenclature

SKA—Squared Kilometre Array.

KAT—Karoo Array Telescope.

RFI—Radio Frequency Interference.

ADC—Analog-to-Digital Converter.

DA—Digital Assembly.

LNA—Low Noise Amplifier.

xNTD—Extended New Technology Demonstrator.

UCT—University of Cape Town.

Local oscillator frequency (LO)—Frequency generated by a local oscillator.

SAW filter—Surface Acoustic Waves filter, widely used in mobile and wireless communication.

Superheterodyne receiver—A receiver with its local oscillator frequency is offset by the IF frequency.

VCO—Voltage Controlled Oscillator, control the desired oscillating frequency by an input voltage

IM—Intermodulation distortion products are unwanted spurious signals generated when signals are being fed into a non-linear device.

Chapter 1

Introduction

The Square Kilometre Array (SKA) is an international effort to build a low-noise and highly sensitive radio telescope with an effective collecting area of one square kilometre, which is spread over an entire continent as in Australia, or over several countries as in Africa [6]. It aims to probe the early universe at frequencies between 0.2 to 20 GHz. It is part of a quest to build an advanced radio telescope that will allow us to conduct more in-depth studies of the universe. South Africa has initiated a project, the South Africa Karoo Array Telescope (KAT) to show the international committee of the SKA that South Africa has sufficient technological knowledge and resources to make a contribution to the SKA. KAT is a 1% pathfinder for the SKA project and will be built in the Northern Cape between 2007 and 2009 [37] [10]. The KAT receiver operates in the frequency range of 700 to 1700 MHz, i.e. covering a 1 GHz bandwidth. It consists of twenty parabolic reflectors, each fifteen metres in diameter[37]. More background regarding the KAT project is presented in section 1.1.

Radio astronomical signals from the universe are often contaminated by man-made radio frequency interference (RFI), and their strengths vary greatly from one location to another. Therefore, the South African SKA team performed various RFI measurements at different sites to ascertain their technical suitability for building the KAT telescope. In the presence of strong interference, the use of a filter in the front-end can prevent such interference, but it will also reduce the sensitivity of the receiver. It is therefore important to understand the various trade-offs when designing receivers. Moreover, the RFI environment must be correctly predicted when designing a robust receiver, so that it can minimise the effects of interference at the receiver output. The performance of the receiver can be evaluated by theoretically predicting certain parameters; this is discussed in Chapter 2.

1.1 Background

Distant celestial objects emit signals that are very weak. Thus it is crucial in radio astronomy to build a highly sensitive radio telescope. The performance of the radio telescope can be improved if a low noise system is implemented. System noise is mainly gener-

ated by the circuitry in the receiver's electronic components. Engineers strive to minimise such noise by using low-noise electronic components. In modern radio astronomy instrumentation, the use of Heterojunction Field Effect Transistor (HFET) amplifier receivers, Superconductor-Insulator-Superconductor (SIS) mixer receivers [26] and cryogenic InP Low Noise Amplifier (LNA) [6] demonstrate improvement in noise performance. Thus it is important to choose the appropriate components to minimise receiver noise.

The South African KAT project aims to show that South Africa has the necessary technological knowledge and sufficient resources to make a contribution to the SKA. The interrelation of the principal components of the KAT system under study in this research is shown in Figure 1.1. The system consists of twenty parabolic dishes, each with a diameter of 15m. These parabolic dishes are based on phased array technology, and each of the antenna dishes reflects the radio power from the radio objects onto its antenna feed, whereafter the signal goes through to the central radio frequency (RF) system. These twenty parabolic dishes are not part of the KAT system discussed in this dissertation, but is for the final KAT system in the future. The KAT system that is being investigated in this dissertation consists of twenty-four front-end LNAs at each of its feed points, which perform pre-amplification; the amplified signal is then fed into the main RF receiver with twenty-four channels. The 24-channel RF receiver has an operating frequency range from 0.7 to 1.7 GHz and supply a power level of -1 dBm at each receiver output channel. This output signal is sampled by the digital assembly (DA) unit. The DA consists of a motherboard that supports six Analogue-to-Digital Converter (ADC) modules. Each ADC module in turn contains a Field Programmable Gate Array (FPGA) and four 10-bit ADC's. The raw ADC data is captured and stored in the internal memory. In-Phase (I) and Quad-Phase (Q) values for all twenty-four RF channels are then computed and integrated over a pre-set number of samples. More information on the DA prototype can be found in [35]. The two 3x4 Vivaldi array of twelve dual polarised elements each (i.e. 2x3x4 channels) requires the twenty-four channels RF receiver in order to carry out tests. This project is intended to allow for the testing of just the two arrays. The real array for the final KAT system is to be 10x10, needing 200 channels.

One of the main concerns of the KAT system is the design of the antenna feed. In order to provide a test bed for evaluating the KAT feed system, both the horn cluster feeds and the focal plane array feeds (FPAs) are being developed by EMSS Antenna (Pty) Ltd and SAAB Grintek (Pty) Ltd respectively. Grintek (Pty) Ltd chose to use the 3x4 Vivaldi antenna array as the radiating element for the FPA because of its excellent broadband operation and its ability to be meshed closely in the arrays [11]. In order to carry out the tests on the 3x4 focal plane array, it is necessary to build a 24-channel RF receiver to test the performance of the array as a receiver. This is the objective of this research, namely to test a 24-channel RF receiver, which has been integrated by Tellumat (Pty) Ltd with suitable local oscillators, power splitters, and receiver controller, which provides the KAT team with a suitable radio receiver to test the two 3x4 dual polarised Vivaldi antennas array. The receiver design and modules were a prototype of the cancelled projected called

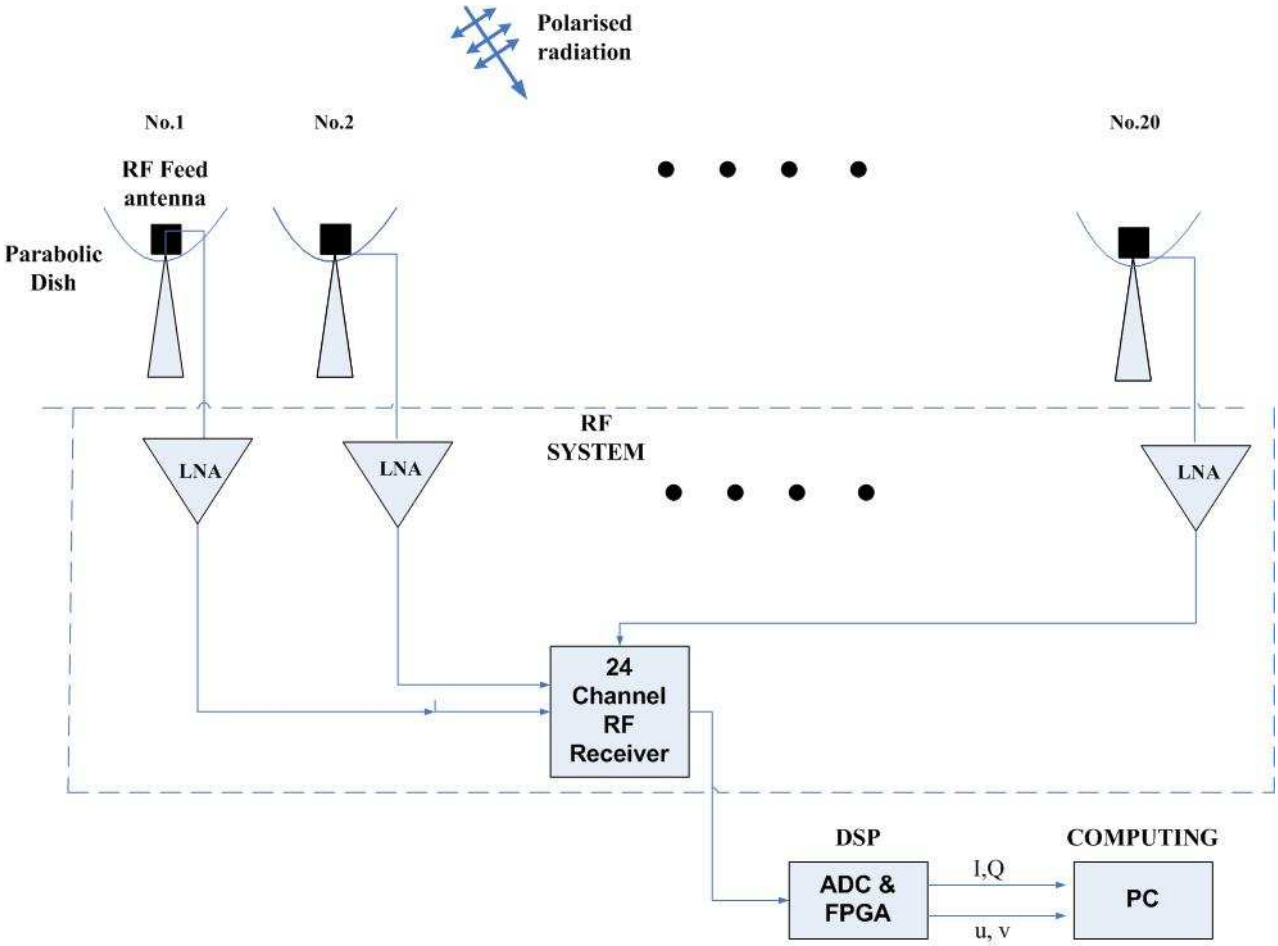

Figure 1.1: Demonstration of the overall KAT system being studied in this research with twenty parabolic dishes and LNAs. The amplified signals from the LNAs are sent through to the 24 channel RF receiver. The output of the receiver is then sampled by the Digital Signal Processing (DSP) unit.

the Extended New Technology Demonstrator (xNTD) project from Australia [5]. The xNTD system specifications are very similiar to those of the KAT, and it therefore provides the perfect opportunity for the KAT team to work in collaboration with the xNTD team. Throughout this dissertation, the receiver module under investigation is referred to as the 3x4 receiver module instead of the KAT receiver module. This is because the 3x4 receiver module is not intended to be used in the final KAT radio telescope system, but is developed to serve as a testing system for the Vivaldi antenna arrays and that the system can be re-used for other application in the future.

1.2 The Objectives of the Research

The objectives of the research are:

1. To provide the background of the KAT project, and explain how it relates to this research.
2. To describe the Australian designed 3x4 receiver module and to predict theoretically its performance by studying all the possible performance parameters of the receiver as a whole.
3. To simulate the design of the 3x4 receiver module using SystemView.
4. To explain the building process of the 24-channel RF receiver integrated by Tellumat (Pty) Ltd and outline the issues needed to be checked during the integration by conducting acceptance tests.
5. To analyse and compare the simulation and acceptance tests results and to determine if the simulator does correctly predict the performance of the 3x4 receiver module.
6. To draw conclusions and make recommendations about the research.

This dissertation thus investigates and evaluates the performance of the Australian built 3x4 receiver module through both simulation and laboratory acceptance tests. By thoroughly understanding how to simulate the existing receiver design using SystemView, one can determine if the simulator can predict the real behaviour of the receiver and hence to conclude if the simulator is reliable. The laboratory acceptance tests setup and data capturing were conducted both at Tellumat (Pty) Ltd and at the University of Cape Town (UCT), and these results were recorded for further data analysis in Chapter 5.

1.3 System Architecture

The planned receiver consists of a front-end antenna and a front-end low noise amplifier (LNA); the RF section then up-converts the RF signals to 3.484 GHz with a bandwidth

of 250 MHz. Thereafter, the signal is then down-converted to an intermediate frequency (IF) of 70 MHz with a bandwidth of 24 MHz. The IF frequency is chosen to be at 70 MHz is because of the low cost SAW filters available from telecommunication industry. Before this down-conversion is performed, the signal is attenuated by the 6-bit programmable attenuator which adjusts the power level of the signals as appropriate to avoid overloading the system if large signals are being detected by the telescope. Thus, in the 3x4 receiver design, an approach called a dual-conversion superheterodyne architecture has been adopted to push the image frequencies up to 4.968 GHz. This avoids the image frequencies that are known to be contaminated by high levels of RFI falling within the receiver band. After the IF signal has been down-converted, it goes through IF post-amplifications to ensure that the signal level has been amplified enough to be able to record amplitude and phase information. The IF output at 70 MHz of the receiver is then fed into an appropriate ADC for digital signal processing.

1.4 Plan of Development

This dissertation presents the 3x4 receiver module design and discusses the trade-off studies conducted during the characterisation of the receiver. The document is structured as follows:

Chapter 2 analyses the design of the 3x4 receiver module from xNTD Project. To meet the aim of designing a highly sensitive receiver, the 3x4 receiver module requirements are defined. The prototype of the 3x4 receiver module adopted from the Australian xNTD project is primarily used for radio astronomy observation purposes. It employs the dual-conversion superheterodyne receiver architecture and the signal received is processed through the two stages of frequency conversion. The effect of noise is one of the most important parameters to consider when designing a highly sensitive receiver. Therefore different possible performance considerations such as receiver gain, signal-to-noise ratio, noise figure, dynamic range, and minimum detectable signal level of the receiver are addressed. All the important component parameters of the 3x4 receiver module are discussed. And by conducting studies on the architecture of the 3x4 receiver module, theoretical predictions of the performance of the 3x4 receiver module are also presented in this chapter. It is not the intention of this research to modify the 3x4 receiver module, but rather to verify that the given design is viable for the integration of the 24-channel RF receiver and that it can be re-used for other application in the future.

Chapter 3 describes the simulation of the 3x4 receiver module by using the time-domain RF simulator SystemView. The components used within the receiver are closely investigated in this chapter, and the choice of these components is explained. The aim of this chapter is to turn the design of the 3x4 receiver module into a simulation, as well as to confirm that the simulation tool is reliable and that it can reflect the real behaviour of the 3x4 receiver module. Certain parameters of the components that are missing due to the

limitations of the simulator are discussed in this chapter.

Chapter 4 presents an overview of the design for the 24-channel RF receiver rack and the 25-channel Calibrator integrated locally by Tellumat (Pty) Ltd. The 24-channel RF receiver consists of twenty-four individual 3x4 receiver modules, two local oscillator boards for the two stages of frequency conversion, and a rack controller. The design trade-offs together with explanations of the functionality of the rack, power supply, local oscillators and rack controller are given in this chapter. Moreover, the complete system block diagram of the RF rack is demonstrated and the functional relationships between the RF rack and its subsystems are discussed. The 25-channel calibrator used to calibrate the receiver modules before use with the antennas is also considered. Lastly, problems encountered during the integration are reviewed.

In Chapter 5, the performance of the 24-channel RF receiver rack is evaluated by means of laboratory acceptance tests on it. This chapter details the acceptance tests carried out on the RF rack by the client (KAT) on the RF rack, with the acceptance tests carried out by the contractor (Tellumat (Pty) Ltd) presented in Appendix A. The contractor was provided with built and tested receiver modules and two motherboards by the client. The responsibility of the contractor was to integrate the subsystems into the rack by providing the two local oscillators mentioned in the summary of Chapter 4 above. The client carried out further tests at the University of Cape Town (UCT) on the RF receiver rack to ensure that it meets the specifications required to be able to test the Vivaldi antenna arrays. These acceptance tests included receiver gain stability, harmonic spurious signals, dynamic range, and two-tone third-order intermodulation distortion measurements, all of which were done for all twenty-four channels of the receiver. The IF output of the receiver at 70 MHz for each channel was checked to ensure that it was as free of spurious signals as possible. The purpose of each of the acceptance tests, the procedures used and the results obtained are explained. Then comparison between simulated and measured results are analysed and presented.

Chapter 6 concludes that the Australian designed 3x4 receiver module is viable to be used in the integration of the 24-channel RF receiver. The resulting theoretical simulations of the 3x4 receiver module using SystemView predicts the real behaviour of the 24-channel RF receiver. It is also shown that, based on the acceptance test measurements, the 24-channel RF receiver integrated by Tellumat (Pty) Ltd has met the design requirements as specified by the client (KAT).

Chapter 2

Receiver Design

The aim of this project is to study and test the design of a 24-channel RF receiver to evaluate a 3x4 Vivaldi antenna array for the KAT project. In order to design a highly sensitive receiver, the overall receiver requirements must be defined. A top-down receiver design methodology and receiver level plan are thus used as planning tools to ensure that the specified design goals have been achieved. It is thus necessary to summarise some fundamental principles of radio receiver design including different receiver architectures and choice of components of the receiver. The effect of noise is one of the most important parameters to consider when designing a highly sensitive receiver. As a result, we will briefly look at considerations such as signal-to-noise ratio, noise figure, dynamic range, and minimum detectable signal level in this chapter.

2.1 Receiver Prototype Requirements

A receiver is used to process the incoming signal and transform it into useful information for data analysis at the digital back-end. When defining the requirements of the receiver, it is crucial to first recognise the specific type of operation that the receiver is intended to perform because various receiver configurations necessitate different performance criteria [43]. The 3x4 receiver module can be depicted as a black box, as shown in Figure 2.1. All possible sources of input signals are identified, including the unwanted noise and interference that appears at the output of the receiver. Certain design aspects for the 3x4 receiver module must be met in order for it to be feasible, and these include the following:

- For the output signal to be useful, the required minimum signal-to-noise ratio (SNR) at the receiver output must be specified, which ensures that the signal power is not embedded in the noise power in order to achieve the most receiver sensitivity;
- Saturation of the receiver when large RFI signals are being received, must be avoided;
- Unwanted out-of-band signals need to be identified and reduce to its minimal to increase receiver sensitivity.

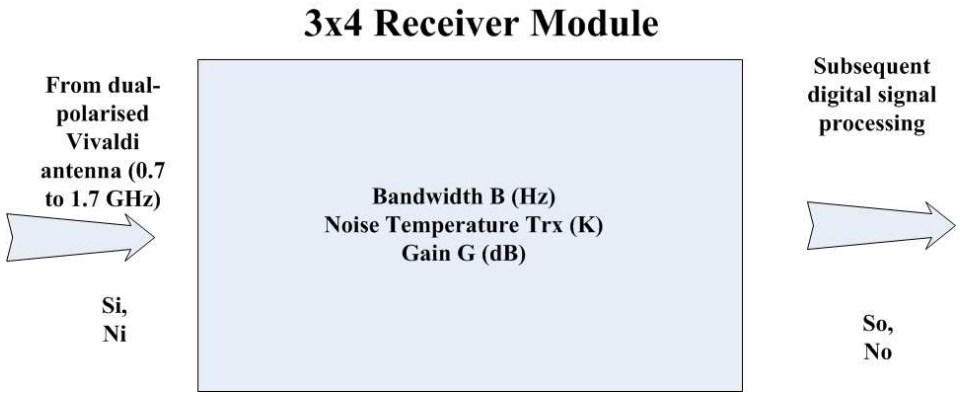

Figure 2.1: Black Box Diagram of the 3x4 Reciever Module

2.2 Dual-Conversion Superheterodyne Receiver

The superheterodyne receiver is the most commonly used receiver architecture still in use today. It is utilised in many commercial applications including tracking radar, telecommunication systems, and radio and television broadcasting systems [38]. The superheterodyne receiver is similar to that of the homodyne receiver, except that the LO frequency (f_{LO}) is offset by the IF frequency (f_{IF}) and is defined as [27]

$$f_{LO} = f_{RF} \pm f_{IF} \tag{2.2.1}$$

For a receiver that operates in higher frequencies (e.g. in the microwave and millimeter frequency band), a second heterodyning stage is needed to translate the frequency down to a lower IF frequency [38]. Two stages of frequency translation (double frequency translation) are needed because it is difficult to perform image frequency rejection if the input signal frequency is higher than the final IF frequency. Receivers with two stages of frequency translation are called dual-conversion superheterodyne receivers. The THousand Element Array (THEA) project from the Netherlands also makes use of the dual-conversion superheterodyne concept for their design of the analog receiver for the SKA [41]. The 3x4 receiver module also employs this receiver architecture which its two stages of frequency translation are discussed in Section 2.3. Despite its advantages, one of the problems of this architecture is having multiple stages of frequency conversion scheme leads to the fact that multiple LOs are required and that increases the spurious signal generated from the non-linearity nature of LOs [27]. Another short-coming is that it generates an undesired image frequency signal during the two stages of heterodyning. This image frequency (f_{IM}) can, however, be separated from the RF signal by a difference equal to twice the IF signal and is given by [32]

$$f_{IM} = f_{RF} - 2f_{IF} \tag{2.2.2}$$

There are two main ways of resolving the image frequency problem. One of the solutions

is to choose a first IF frequency that is as high as possible because the image frequency is separated from the RF signal twice the IF frequency and, when using a high first IF frequency, the receiver has the ability to reject this. The other solution is to use a band-pass filter before the mixer and thus before heterodying takes place, which also helps to suppress the image frequency [38]. Another issue to consider is the choice of the second IF frequency. This determines the selectivity of the receiver [32].

2.3 Receiver Prototype Description

The prototype of the 3x4 receiver module adopted from the Australian xNTD project is primarily used for radio astronomy observation purposes. As shown in Figure 1.1, the first stage of the KAT system consists of a front-end LNA, followed by the 3x4 receiver module. The input signal is picked up by the antenna and sent to the front-end LNA. This is the first component of the KAT system, and it plays an important role in determining the overall noise figure, as the overall noise figure of a cascaded system is dominated by its first component, and as the subsequent stages will have less effect on the overall noise figure [27]. The overall noise performance of a cascaded system thus depends on the first component, which means that this component must have a low noise figure and preferably a high gain. It is thus not ideal to use a filter in front of the LNA; although a filter prior to amplification can prevent interference, it also reduces the sensitivity of the receiver [29]. In radio astronomy application, the typical gain of the front-end LNA is about 20 to 25 dB with a noise temperature of 50K [17]. Additional investigation of the choice of the front-end LNA is beyond the scope of this research, hence the study only looks at the 3x4 receiver module.

The 24 channel receiver consists of twenty-four individual 3x4 receiver modules. The signal received is processed through a dual-conversion superheterodyne receiver module as shown in Figure 2.2. This receiver module consists of two sections:

- The RF Section consisting of one stage of up-conversion from the RF reception band to the first IF at 2.484 GHz and a 6-bit programmable attenuator with variable attenuation from 2 to 31 dB;
- The IF Section consisting of the second stage of down-conversion from 2.484 GHz to a fixed second IF frequency at 70 MHz with the IF bandwidth of 24 MHz. Thereafter it goes through a number of narrow-band IF Surface Acoustic Waves (SAW) bandpass filters and IF amplifications.

2.3.1 RF Section

In the RF section as shown in Figure 2.3, the signal is amplified further by an amplifier with a gain of 15 dB. The amplified signal goes through the preselect bandpass filter with a

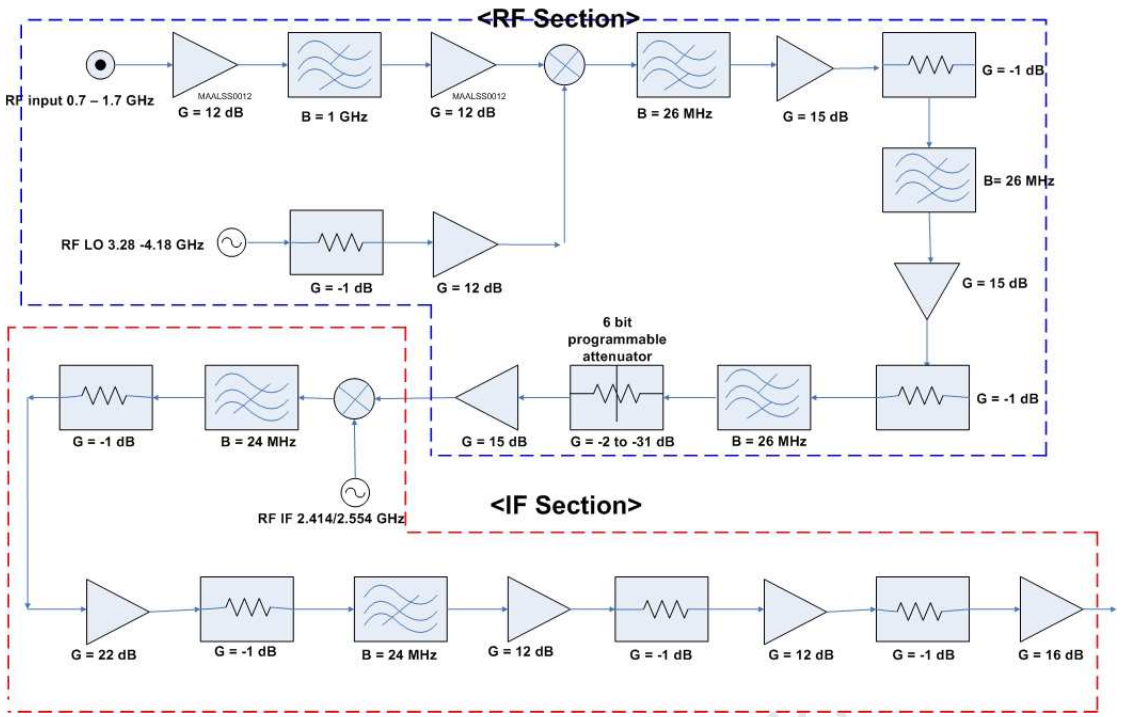

Figure 2.2: Block diagram of the 3x4 Receiver Module

bandwidth of 1 GHz (i.e. from 0.7 to 1.7 GHz) which filters out the undesired out-of-band interference. The signal then goes through an amplifier with a gain of 12 dB to increase the power level of the signal before it enters the first mixer of the receiver chain. This signal is then up-converted from the RF reception band to 2.484 GHz by a variable local oscillator (RFLO). The variable RFLO converts the RF signal which lies in the operation band to the first IF (IF1) at 2.484 GHz. Figure 2.4 illustrates this up-conversion process.

This IF1 was chosen because the image frequency is rejected more effectively with a high IF frequency, as the image frequency will be much further away from the desired signal. Figure 2.5 shows how far away the image frequency is from the desired signal and how it is filtered out. After the up-conversion, the output from the mixer is applied to a number of filtering and amplification stages with 1 dB attenuators in between to improve the match. Filters decrease the sensitivity of the receiver module and thus it is often useful to distribute the filters into a number of stages with amplifiers combined in between to reduce the effects of filter losses before the signal enters the IF section for the next stage of frequency translation [32]. A filter-amplifier-attenuator configuration is employed to ensure minimal distortion [17]. In some receiver designs, an automatic gain control (AGC) amplifier is used to adjust the power level of the signal accordingly to avoid the signal from overloading the receiver. Instead, for the 3x4 receiver module design, a 6-bit programmable attenuator with an attenuation that varies from 2 to 31 dB is achievable, and it allows the user to adjust the suitable power level before the signal enters the IF section.

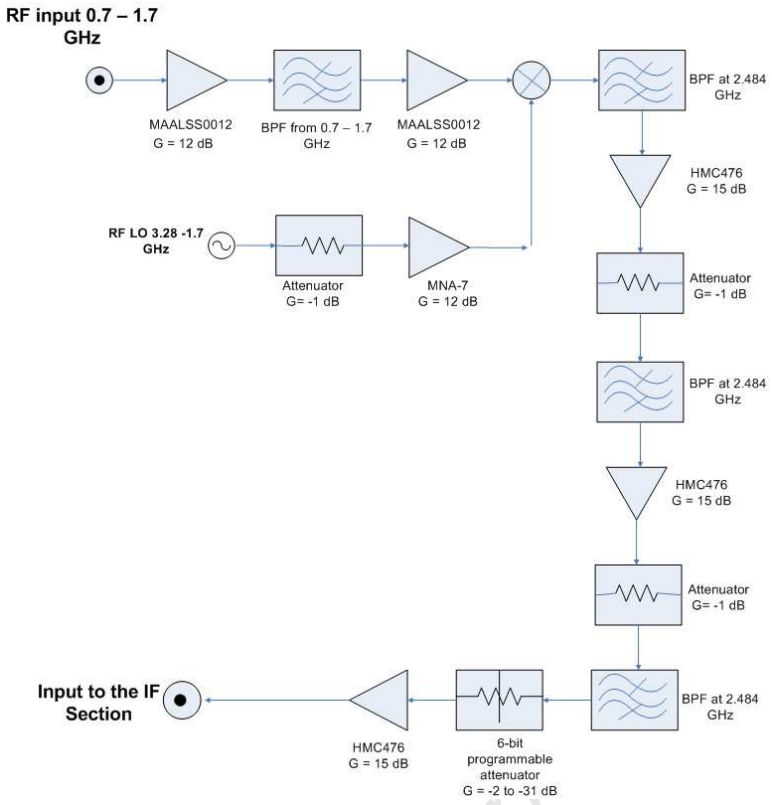

Figure 2.3: RF Section of the 3x4 receiver module

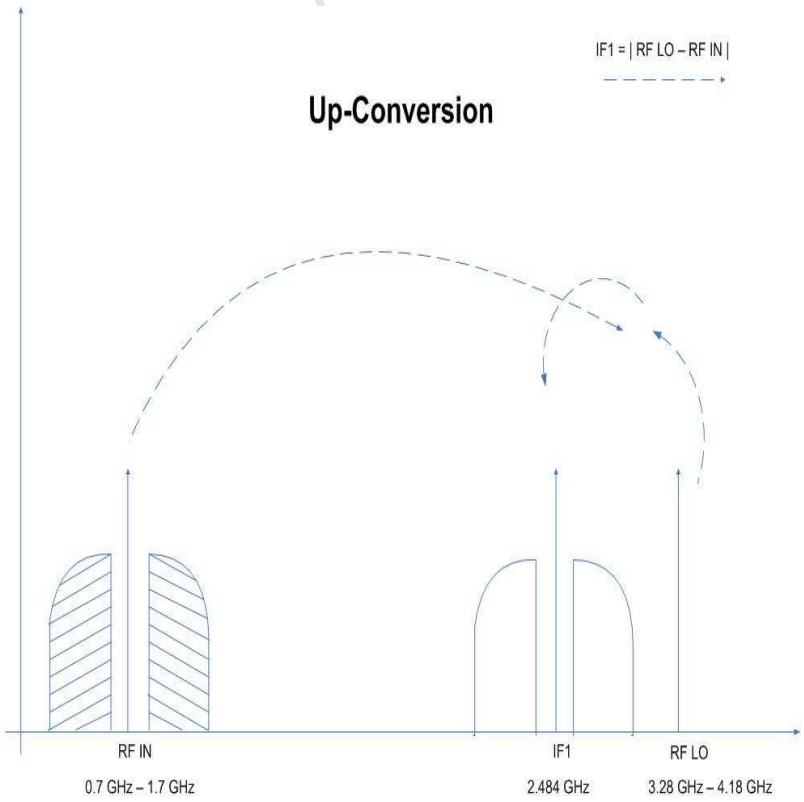

Figure 2.4: Up-conversion in the RF section of the 3x4 receiver module

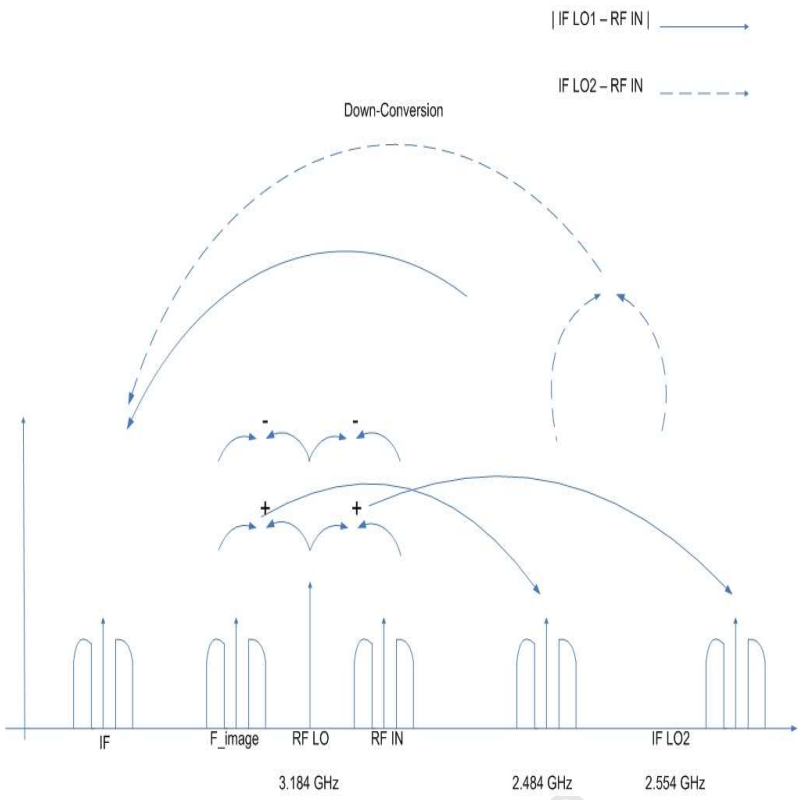

Figure 2.5: Filtering of the image frequency by performing up-conversion

2.3.2 IF Section

In the IF section, as shown in Figure 2.6, the IFLO is designed to have two fixed LO frequencies (referred to as IF LO1 at 2.414 GHz and IF LO2 at 2.554 GHz). If IF LO1 is chosen, the IF will be in the positive spectrum at + 70 MHz and for the IF LO2, IF will be in the negative spectrum at - 70 MHz. The output from the RF section is applied to the second mixer and the signal is down-converted to the second IF frequency (IF2) to 70 MHz and the IF signal gets bandpass filtered by the IF SAW filters with a bandwidth of 24 MHz, as shown in Figure 2.7. The IF2 frequency of 70 MHz is a standard telecommunication frequency, and a lower IF frequency was chosen to improve the channel selectivity because of its IF narrow bandwidth and high out of band rejection [40]. In addition, the choice of this IF frequency is determined by the low cost of SAW filter for wireless local area network (LAN) market [3]. Post-amplification only happens after the down-conversion because the stability of amplifer gain can easily be achieved at low frequency [32]. The IF output of the IF section at 70 MHz with a power level of -1 dBm is applied to the ADC unit for digital signal processing.

2.4 Receiver System Parameters

As presented in the previous section, the receiver system parameters directly affect the performance of the receiver, the following parameters are discussed:

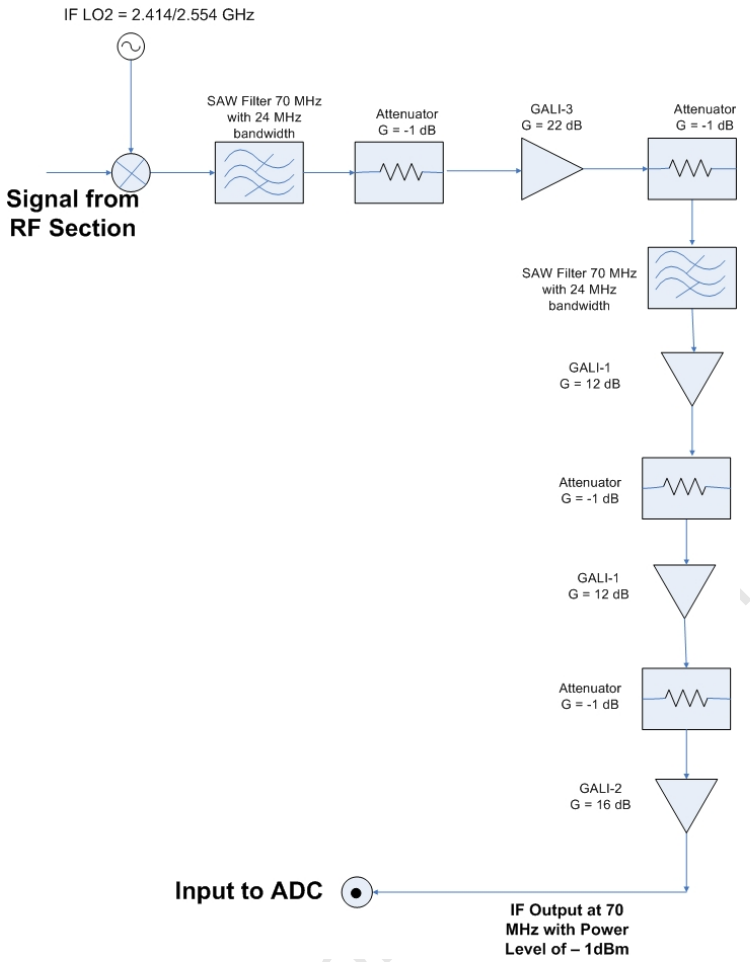

Figure 2.6: IF Section of the 3x4 receiver module

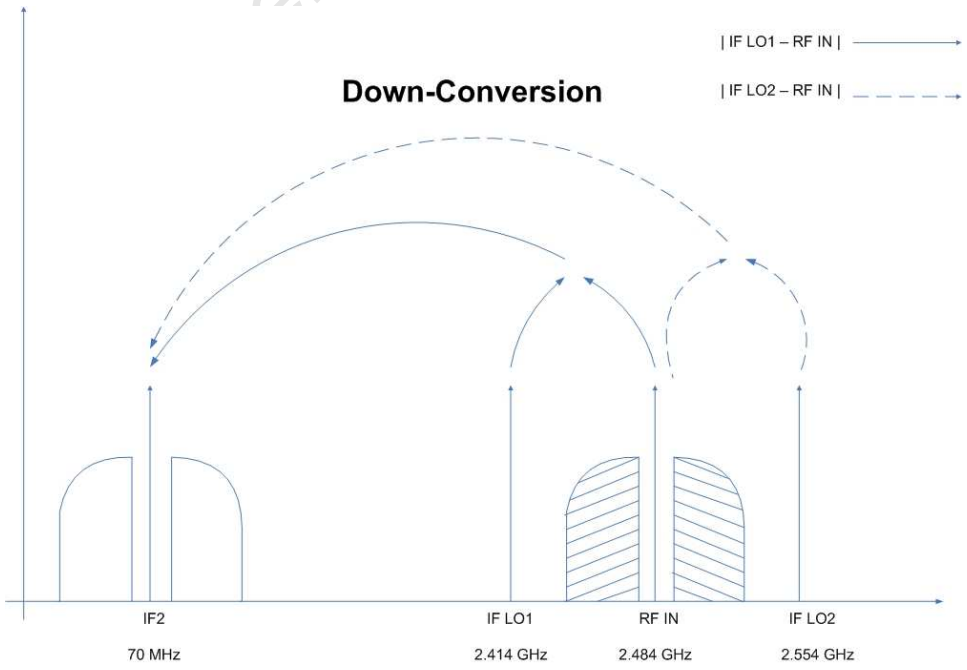

Figure 2.7: Down-conversion in the 2^{nd}stage of mixing to a IF frequency of 70MHz

- Gain
- Noise figure and equivalent noise temperature
- Sensitivity
- 1dB Compression point
- Harmonic distortion and Intermodulation distortion
- Dynamic range

2.4.1 Gain

Receiver gain can be described as the ratio of the output and the input power level of the receiver, and is expressed in dB [32]. The amount of gain provided by the receiver must be sufficient to increase the power level of the desired signal at the receiver output, which prevents the receiver noise from dominating the measured signal [42]. The overall gain (G_{rx}) of the receiver can be calculated if the output noise power at the receiver, N_o, is specified [41]

$$G_{rx} = \frac{N_o}{k(T_a + T_e)B} \tag{2.4.1}$$

The signal path of the 3x4 receiver module is depicted in Figure 2.8.

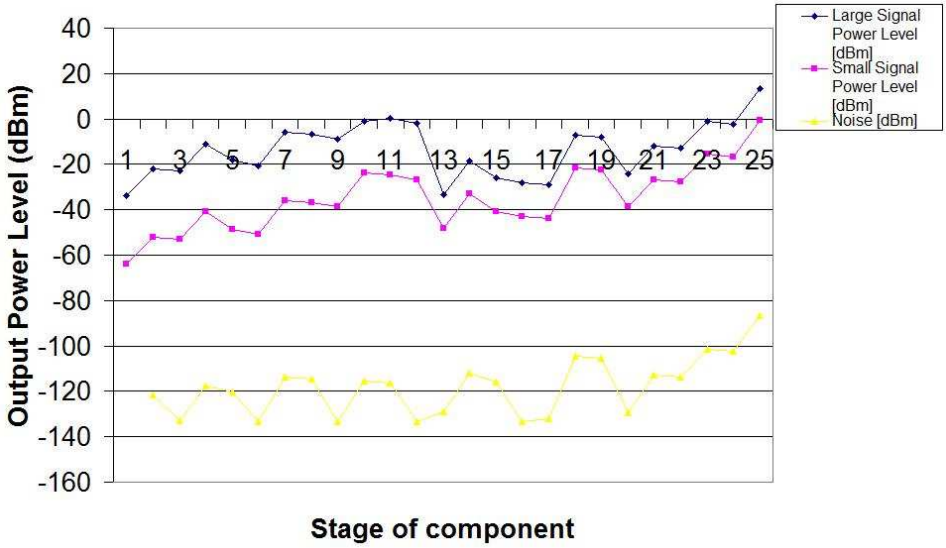

Figure 2.8: Maximum and minimum system gain of the 3x4 Receiver module

It is shown that an output power level of -1 dBm is provided at the 3x4 receiver module output, which matches the input power level requirement of the DA unit. The above power tracking graph also shows that the output noise power level of the receiver module varies

from -64 to -34 dBm, given that the overall gain of the 3x4 receiver module ranges from 21 to 50 dB in the RF section and that a fixed gain of 18 dB is achieved in the IF section.

The rule of thumb when designing a receiver is to distribute the overall receiver gain among the various receiver stages and to assign a high gain to the second IF stage. It is important to have an adequate gain before the signal enters the mixer because of its poor noise figure (NF) value. But it is also important to bear in mind that minimisation of power level to the input of the mixer can reduce the power levels of the spurious signals. One has to be cautious when choosing the second IF frequency and should ensure that it is as free as possible from spurious signals, otherwise the unwanted signal will be amplified by the high IF gain and affect the receiver performance [38].

2.4.2 Noise Figure and Equivalent Noise Temperature

The Noise Figure (NF) measured in dB, determines the effect of the receiver on the signal as it passes through the receiver and provides a measure of how noisy the receiver is [7]. NF can be defined as the degradation between SNR_o and SNR_i and it can be expressed as [27]

$$NF = 10\log(\frac{SNR_o}{SNR_i}) \tag{2.4.2}$$

Ideally, one would want to accomplish a NF = 0 dB (or T_e= 0 K). The equivalent noise temperature (T_e) and NF are interchangeable and can be used to characterise the noise properties of the system. T_e is inter-related to the NF as

$$T_e = T_o(F-1) \tag{2.4.3}$$

where F is referred to as Noise Factor, and is just the linear form of NF instead of dB.

In the receiver chain, each component contributes to the overall noise figure of the receiver, with the first component dominating the overall noise figure of the receiver [6] and the subsequent stages of the receiver having less impact on the overall noise figure. Therefore the NF of a receiver with n cascaded components can be calculated using [27]

$$F_{cascaded} = F_1 + \frac{(F_2-1)}{G_1} + \frac{(F_3-1)}{G_1G_2} + ... + \frac{(F_n-1)}{G_1G_2...G_{n-1}} \tag{2.4.4}$$

where F_n and G_n are the noise figure (in linear form) and the gain of the n^{th} component of the receiver respectively. It is important to clarify that, in this dissertation, the first component for the 3x4 receiver module is an amplifier, the front-end LNA (with a gain of approximately 25 dB), which is placed before the 3x4 receiver module and this is

not taken into the account when calculating the overall noise figure of the 3x4 receiver module. The LNA is out of the scope of this dissertation, therefore the objective of this dissertation is just to investigate the 3x4 receiver module excluding the effect by the LNA. By using equation 2.4.4, the overall noise figure of the 3x4 receiver module is NF = 1.9dB with a T_e= 129 K.

In radio astronomy, investigations have been conducted to minimise the overall system noise figure. Chippendale [6] for instance, discusses a number of technological issues regarding the minimisation of the system noise figure by improving the semiconductor process and the feasibility of cooling the receiver to reduce the receiver noise temperature.

Essentially, the higher the noise figure (or noise temperature) of the system, the more noise it adds to the signal. In general, two main types of noise are picked up by the antenna [16], namely natural noise sources and receiver noise.

2.4.2.1 Natural Noise Source

This includes sky noise, earth noise, atmospheric noise, galactic noise and man-made noise. Depending on what the antenna is pointing at, for example, the magnitude of sky noise can differ. The input noise power level for the 3x4 receiver module can be calculated by using equation 2.4.5,

$$N_i = kT_aB \tag{2.4.5}$$

where B is the IF bandwidth of the receiver, k is the Boltzmann's constant, and T_a is the antenna noise temperature. T_a is assumed to have a value of 290K if the antenna pointed to the horizon of the earth [16]. For radio astronomy, the antenna is usually pointing up the sky (i.e. toward zenith). Therefore the actual sky temperature will be about 3 K to 5 K, contributed by the cosmic background radiation. An input noise power level of -118 dBm is thus obtained for the 3x4 receiver module when point at the sky.

Man-made noise has many different sources and depends on the location of the receiver. This type of interference can be minimised by choosing an environment with low RFI. The SKA team has thus chosen a number of sites with low RFI and conducted RFI measurements on these sites. Dunn[1] has been investigating the feasibility of the RFI measurements protocols, and Mngadi [2] has investigated the RFI measurement equipment used for the SKA.

2.4.2.2 Receiver Noise

This is generated internally by the receiver's circuitry and constitutes the noise floor of the system. Receiver noise can be predicted by calculating the SNR. The higher SNR value

[1]Sydney Dunn is currently a masters student at the University of Cape Town.
[2]Andile Mngadi is also a masters student at the University of Cape Town.

should be accomplished because it corresponds to better receiver performance. Different types and causes of receiver noise are discussed in [16].

2.4.3 Sensitivity

Receiver sensitivity is the ability of the receiver to detect the weakest signal [8]. The higher the sensitivity of the receiver, the better its ability to detect faint signals emitted from radio sources. The sensitivity of a receiver is bandwidth dependent, meaning that as the bandwidth of the receiver becomes wider, more noise passes through to the output and reduces the sensitivity of the receiver. Another parameter that limits the sensitivity of the receiver is its noise floor, which is generated internally by the receiver's circuitry, and which can be associated with the noise figure of the receiver. Receiver sensitivity can therefore be expressed by using equation 2.4.6

$$S_{min} = SNR_{min} T_o k B F \tag{2.4.6}$$

where SNR_{min} is the minimum SNR or signal plus noise and distortion-to-noise and distortion ratio (SINAD). It can be calculated by using the equation below

$$SINAD = 1 + SNR \tag{2.4.7}$$

2.4.4 1 dB Compression Point

The 1 dB Compression Point (P1dB) sets the limit of the largest signal the system can handle without becoming saturated [28]. As the power level of the input signal that goes into the components (amplifier, mixer or receiver) is less than the input 1 dB compression point, the output will be proportional to the input without becoming saturated. If the signal exceeded the 1 dB compression point, the output signal no longer operates in the linear region and unwanted spurious output signals called intermodulation distortion products (IM) are generated as a results.

2.4.5 Harmonic Distortion and Intermodulation Distortion

As described in Section 2.2, one of the major problems of the superheterodyne receiver is the generation of spurious signals due to multiple LOs used for the double frequency conversion. When a single-tone signal f_1 (fundamental) is fed into a non-linear device, harmonic distortion products are generated at the frequencies

$$M f_1 \quad where \quad M = 1, 2, 3... \tag{2.4.8}$$

Harmonic distortion is measured in dBc, which uses the carrier (fundamental) frequency as a reference [24].

IM are generated when one or more signals are fed into a non-linear device. IM can be predicted by conducting a two-tone test, which will be discussed in Chapter 3 in more detail. If two closely spaced input signals f_1 and f_2 are fed into a non-linear device, the frequencies of the IM occur at

$$mf_1 \pm nf_2 \quad where \quad m, n = 0, 1, 2, 3... \tag{2.4.9}$$

The sum of $|m| + |n|$ defines the order of the intermodulation products. The 2^{nd} and 3^{rd} order intermodulation products would occur at the frequencies as shown in Table 2.1.

Type of Intermodulation Product (IM)	Frequency
2^{nd} order	$f_1 + f_2$; $f_1 - f_2$; $2f_1$; $2f_2$
3^{rd} order	$2f_1 + f_2$; $2f_1 - f_2$; $f_1 + 2f_2$; $f_1 - 2f_2$

Table 2.1: 2^{nd} and 3^{rd} order intermodulation distortion products freqencies.

The third-order intercept point (IP3) is where the first order and third order powers intersect [27]. It is common in practice to say that IP3 is 10 to 20 dB greater than P1dB, assuming the input power level is at the same reference point. The input P1dB (P1dBin) can be determined if IP3 referred to the input is given [20]

$$P1dB_{in} \quad = \quad IIP3 - 9.6dB \tag{2.4.10}$$

The aim is to achieve a high overall IP3 value for a high performance receiver. However, cascading the components together will degrade the IP3 point. Therefore the distortion of the IP3 power for a cascaded system with n components can be calculated [16] by:

$$\frac{1}{OIP3} \quad = \quad \frac{1}{\frac{1}{OIP3_1} + \frac{1}{OIP3_2 G_1} + \frac{1}{OIP3_3 G1G2} + ... + \frac{1}{OIP3_n G_1 G_2 ... G_{n-1}}} \tag{2.4.11}$$

where $OIP3_n$ is the output IP3 of the n^{th} component in the receiver chain and G_n is the gain of the n^{th} component.

2.4.6 Dynamic Range

The dynamic Range (DR) of a receiver is defined as the linear operating region of a receiver, and it is set by the 1 dB compression point of the system [44]. It can also be interpreted as a measure of the ratio between the strongest and weakest input signal a

receiver can handle, given the minimum detectable signal (MDS) in decibels [32]. The MDS or minimum acceptable signal level in a receiver is affected by the internal noise of the receiver. It is usually defined to be 3 dB above the noise floor of the receiver [16]

$$MDS = N_i + 3dB \tag{2.4.12}$$

Using equation 2.4.12, the MDS level of the 3x4 receiver module, referred to the receiver input is calculated to be -115 dBm. N_i will be substituted by N_o , if MDS referred to the output is to be calculated.

The receiver performance parameters for determining the dynamic range of the receiver can be measured by looking at the IM levels. Good receivers usually have a DR of at least 100 dB [36]. If a receiver has limited dynamic range, its actual performance is reduced.

Knowing the MDS of the receiver and P1dB of the system, the dynamic range, in dB, can be calculated as [8]

$$DR = IIP1 - MDS \tag{2.4.13}$$

where IIP1 is the P1dB referred to the receiver input in dB.

Using the equation 2.4.13, the calculated dynamic range of the 3x4 receiver module is 122.78 dB.

Spurious-free dynamic range (SFDR) is another way of characterising the receiver performance. SFDR is the receiver dynamic range when two input signals with equal power levels are applied to the receiver, where there is no 3^{rd} order IM response exceeding the MDS level [44]. It can be expressed as

$$SFDR = \frac{2}{3}(OIP3 - MDS) \tag{2.4.14}$$

where OIP3 is the 3^{rd} order intercept point at the output of the receiver. Figure 2.9 shows the linear operating range of the 3x4 receiver modules from the calculated values using the above equations.

2.4.7 Conclusion

In this chapter, the fundamental design principles of the 3x4 receiver module including its architecture and choice of components were discussed. The performance of the receiver is directly affected by different system parameters, and these parameters were investigated in this chapter in terms of theoretical analysis and mathematical calculations. The overall calculated design parameters of the 3x4 receiver module are summarised in Table 2.2.

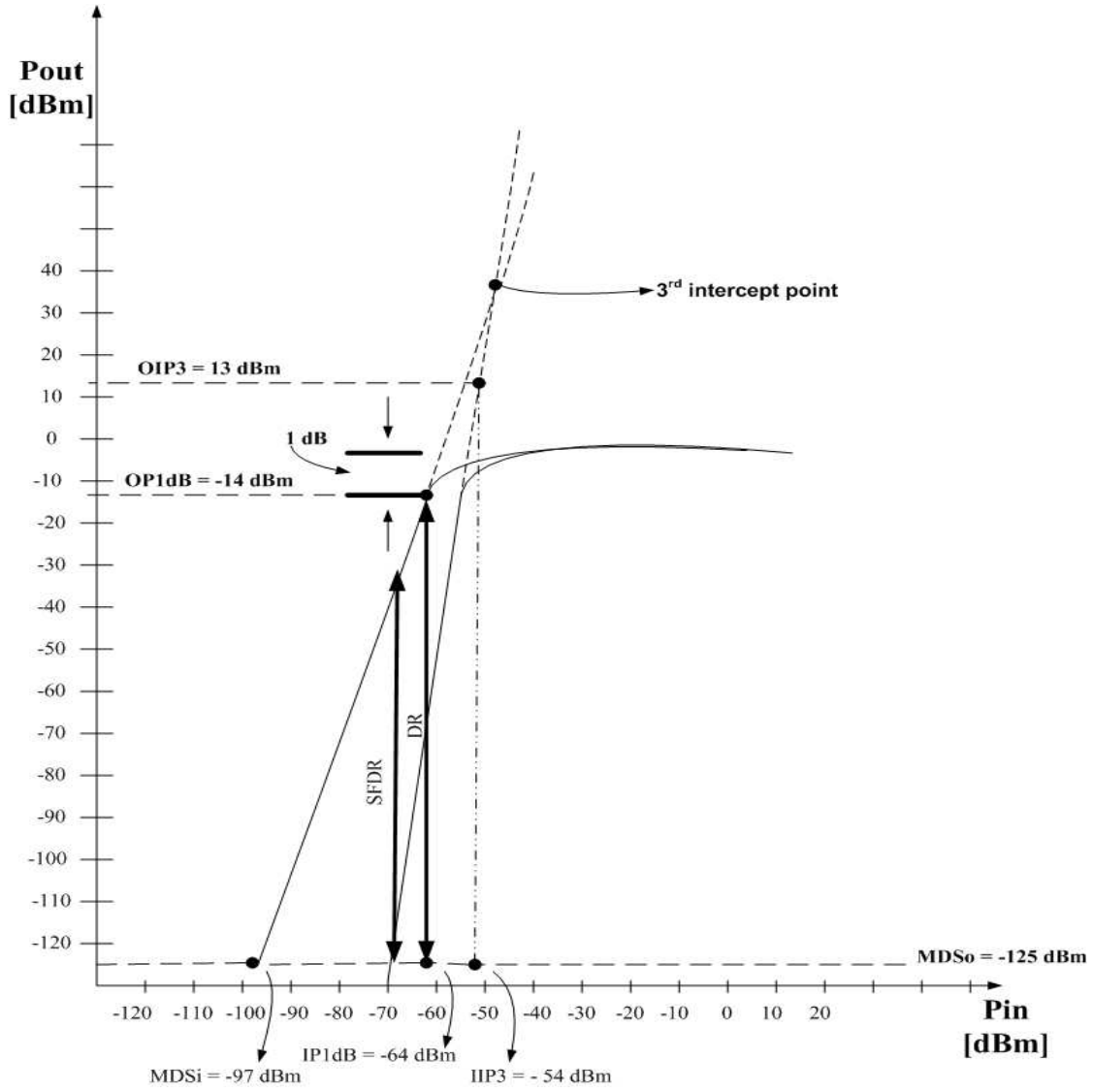

Figure 2.9: Linear dynamic range and spurious free dynamic range of the 3x4 receiver module.

It is found that the 3x4 receiver module has a linear dynamic range of 105 dB, and a system gain varies from 39 to 68 dB. In addition, Table 2.3 shows the level diagram of the 3x4 receiver module with twenty-four stages. The noise figure, system gain and third order intercept point for each stage throughout the receiver are being identified. These parameters must be thoroughly understood and will thus be discussed further in the next chapter, to assist with the simulations in Chapter 3 of the 3x4 receiver module using SystemView.

Parameter	Value
Linear Dynamic Range (DR)	122.78 dB
Spurious-free Dynamic Range referred to the input ($SFDR_i$)	49 to 68 dB
Spurious-free Dynamic Range referred to the output ($SFDR_o$)	93 dB
MDS_o	-76 to -47 dBm
MDS_i	-115 dBm
OIP3	14 dBm
IIP3 = OIP3 - G	-54 to -25 dBm
$NF_{cascaded}$	1.9 dB
T_e	162 K
N_i	-118 dBm
N_o	-79 to -50 dBm
S_i	-69 to -40 dBm
$S_{min}$with SINAD 34 dB	-64 dBm
$S_{min}$with SINAD 63 dB	-35 dBm
SNR_odepending on N_o	33 to 62 dB
Input 1 dB Compression Point IP1dB	7.78 dBm
System Gain	39 to 68 dB
SINAD with $N_o min$ (SNR_{min})	63 dB
SINAD with $N_o$max (SNR_{min})	34 dB

Table 2.2: Design parameters for the 3x4 receiver module.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Gain [dB]	+12	-1	+12	-8	-2	+15	-1	-2	+15	-1	-2	-2 to -31	+15	-8	-16	-1	+22	-1	-16	+12	-1	+12	-1	+16
Noise Figure [dB]	1.5	1	1.5	8	2	2.5	1	2	2.5	1	2	4	2.5	8	2	1	3.5	1	2	4.5	1	4.5	1	4.6
OIP3 [dBm]	32	-	32	5	-	25	1	-	25	1	-	41	25	7	-	1	25.3	1	-	15.4	1	15.4	1	19.5

Table 2.3: Level planning diagram of the 3x4 receiver.

Chapter 3

Simulation of the 3x4 Receiver Module

This chapter presents the simulation for the 3x4 receiver module that is conducted in the time-based RF simulator, SystemView[1]. In this chapter, the analysis of the data recorded from the simulation will be discussed. Then explanations for how the simulations were run, with several simulation control elements of each component of the 3x4 receiver module will be specified and indicated. Therefore this chapter aims to evaluate the performance of the receiver through accurate simulations to detect any flaws in the design.

The objective of the simulation is to verify the RF power level dynamic range, spurious signals including intermodulations and harmonics for the 3x4 receiver. The simulation is modelled in such a way that it can predict the behaviour of the 3x4 receiver module as closely as possible. The simulation result is then compared with the actual measurements obtained from the receiver acceptance tests, which will be discussed in Chapter 5.

3.1 Components and Effects of the Receiver Module

SystemView simulates the system by using function blocks, or tokens. The user can characterise the token through setting its parameters provided by SystemView. Figure 3.1 shows the processing tokens of the 3x4 receiver module in SystemView.

The Nyquist's sampling theorem states that the sampling rate (fsampling) of a system must be set to at least twice its maximum system frequency (fmaximum) to avoid aliasing [38],

$$f_{sampling} \geq \ 2 \times f_{maximum} \tag{3.1.1}$$

In SystemView, the sampling rate is advised to be chosen between 3 to 5 times the maximum system frequency [18]. In the 3x4 receiver simulation, a sampling rate of four times the maximum operating frequency is chosen (i.e. fsampling = 20 GHz), which is slightly

[1]SystemView Professional Edition 2005.02 is used for all the simulations in this dissertation.

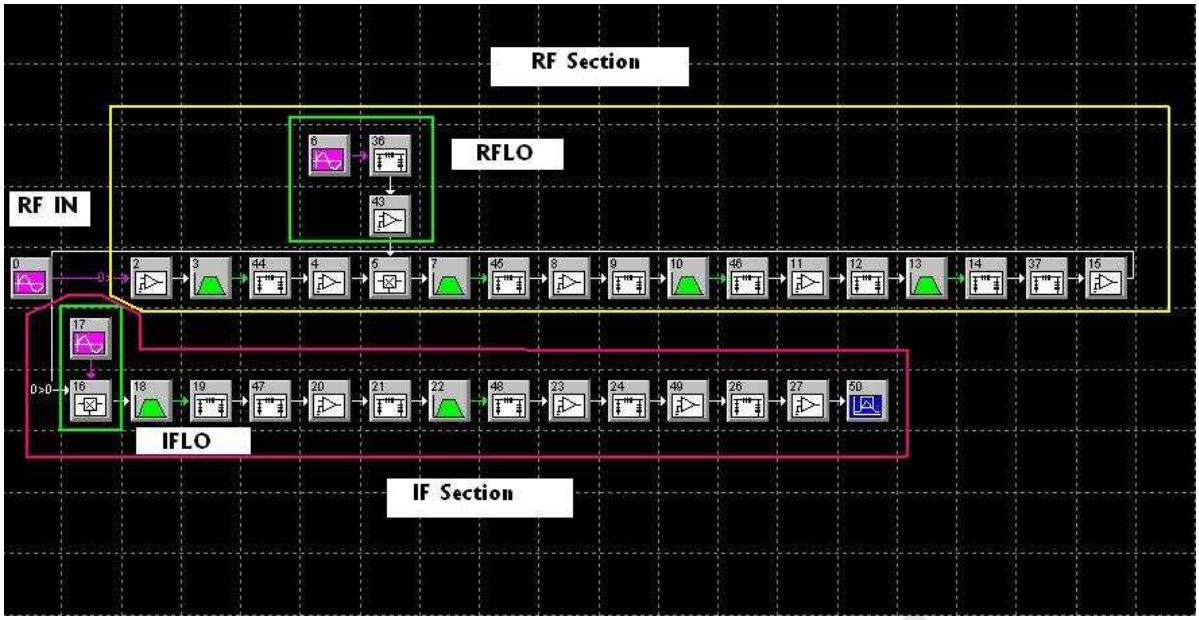

Figure 3.1: 3x4 Receiver Module line-up, divided into the RF section and IF section.

greater than four times the RF maximum frequency with a resolution frequency of 50 kHz. In SystemView, the simulated signal can be decimated at the lower IF frequency in order to reduce the need of computer memory. But this function was not used in the simulation, as it was not required.

The design description of the 3x4 receiver module was discussed in Chapter 2. Therefore this chapter only serves to explain how each of the components of the 3x4 receiver module is being modelled in SystemView. The 3x4 receiver module simulation can be divided into two main sections, namely the RF and IF section, which will be discussed in the following sections.

3.1.1 RF Section

The first component of the RF section is the RF amplifier with a gain of 12 dB. It is important not to saturate the amplifiers by feeding in the appropriate power levels that do not exceed the specified IP3 points of the amplifiers. Certain design parameters including gain, noise figure, OIP3 points and 1 dB compression points are required to be set in the simulation in order to correctly characterise each amplifier used in the 3x4 receiver module. Following the amplifier, is the RF bandpass filter with a passband from 700 to 1700 MHz and is modelled by a three-pole Chebyshev filter in the simulation. Since SystemView do not simulate filter insertion loss, the loss of this RF bandpass filter (2 dB) is simulated by using the fixed attenuation token. The next main component after the RF BPF is the RFLO, which up-converts the RF signal with a variable local oscillator frequency from 3184 MHz to 4180 MHz depending on the RF input signal frequency (Refer to section 2.3.1 for details). The simulation control elements for RFLO mixer are shown in Table 3.1. After going through a number of stages of amplification (for each amplifier

with a gain of 15 dB), bandpass filtering (each filter is a one-pole Chebyshev filter) and attenuation (1 dB fixed attenuators), the signal is being attenuated by the 6-bit attenuator, which is modelled by a fixed attenuator token in SystemView, with attenuation ranges from 2 to 31 dB in 1 dB increment. Refer to Figure 2.3 for component part numbers.

Parameters	RFLO mixer	IFLO mixer
(1) Conversion loss	8 dB	8 dB
(2) Mixer frequency	3.184 to 4.180 GHz	2.414/2.554 GHz
(3) RF port isolation	35 dBc	15 dBc
(4) LO port isolation	17 dBc	15 dBc

Table 3.1: Simulation parameters for RFLO and IFLO mixers.

3.1.2 IF Section

In the IF section, the IFLO can be tuned to a fixed oscillator frequency of 2414 MHz (for positive IF spectrum at + 70 MHz) or 2554 MHz (for negative IF spectrum at -70 MHz. (Refer to section 2.3.2 for details). The simulation control elements for IFLO are shown in Table 3.1. It then follows by a IF SAW filter (one-pole Chebyshev filter) with a bandwidth of 24 MHz, with a center frequency of 70 MHz. A fixed attenuation token is set to 16 dB to compensate the IF SAW filter insertion loss in the simulation. It then follows by a number of IF post-amplifications (with cascaded gain of 22 dB, 12 dB, 12 dB, and 16 dB) and attenuation (1 dB attenuation each) in between, and the output of the IF section corresponds to the IF output of the 3x4 receiver module. Refer to Figure 2.6 for component part numbers.

3.2 Discussion of Simulation Results

The entire 3x4 receiver module simulation results are discussed in this section. Several simulations were performed according to the following conditions:

- RF input power level sweep and receiver gain
- Power level tracking
- Variable attenuation ranges from 2 dB to 31 dB in 1 dB step
- Two-tone test
- Receiver noise

3.2.1 RF Input Power Level Sweep and Receiver Gain

To simulate the receiver gain, an RF input signal with power level ranges within the specified dynamic range (-64 to -34 dBm) is fed into the system, and the IF output power level is then recorded. Figure 3.2 shows the IF output power level of the 3x4 receiver module at 70 MHz, with a input RF signal at 700 MHz, and a maximum power level of -34 dBm. The 6-bit attenuator is set to have an attenuation value of 31 dB. Figure 3.3 shows the IF output of the 3x4 receiver with a minimum input RF power level of -64 dBm at 700 MHz. Table 3.2 gives a summary of IF output power level with varying input power level at 700, 1200, and 1700 MHz and the average gain of the receiver over the operating RF frequency band. Theoretically, a receiver gain between 39 to 68 dB is expected, which agreed with the simulation result.

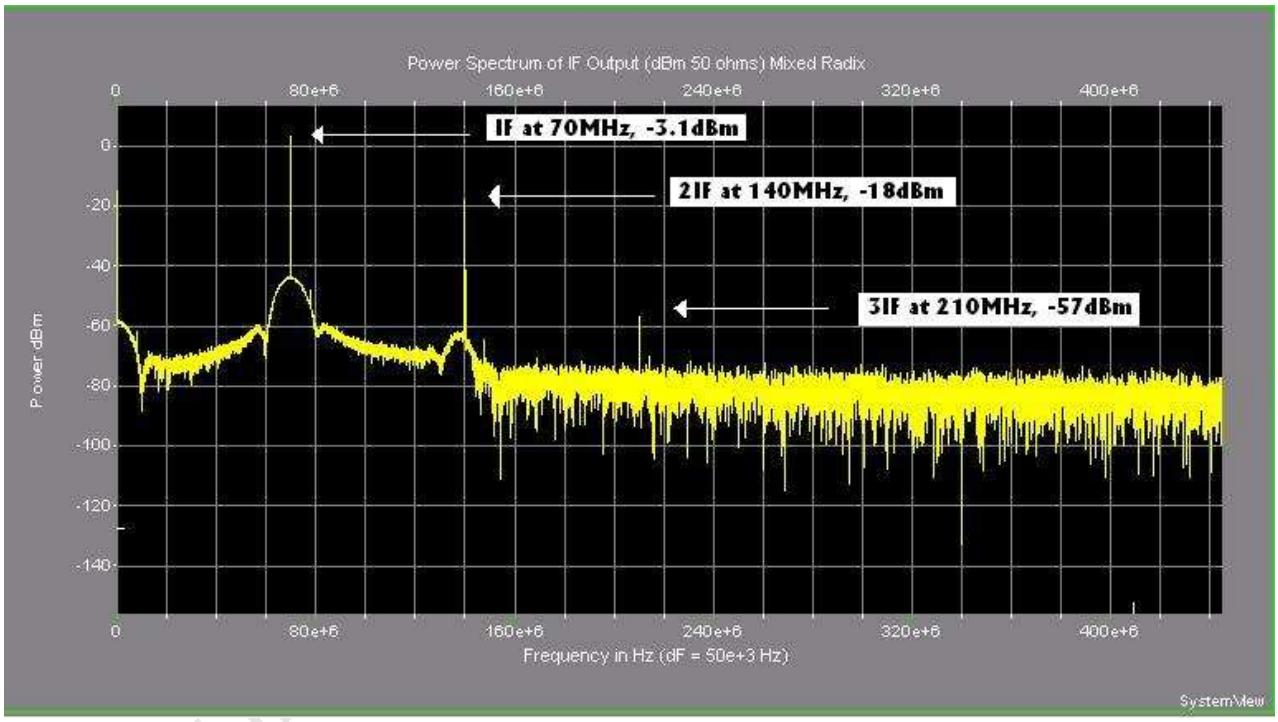

Figure 3.2: IF output of the 3x4 receiver module in SystemView with a maximum RF input power level of -34 dBm at 700 MHz. 2IF is the second harmonic of the IF and 3IF is the third harmonic of the IF.

3.2.2 Power Level Tracking

The output power level for each stage of the 3x4 receiver module is tracked. Figure 3.4 shows the power output level at each output stage of the 3x4 receiver. An RF input signal at 700 MHz with a power level of -50 dBm is injected into the 3x4 receiver, with an attenuation of 18 dB. The output power level at the output of each component from the simulation correspnds to the theoretical calculations.

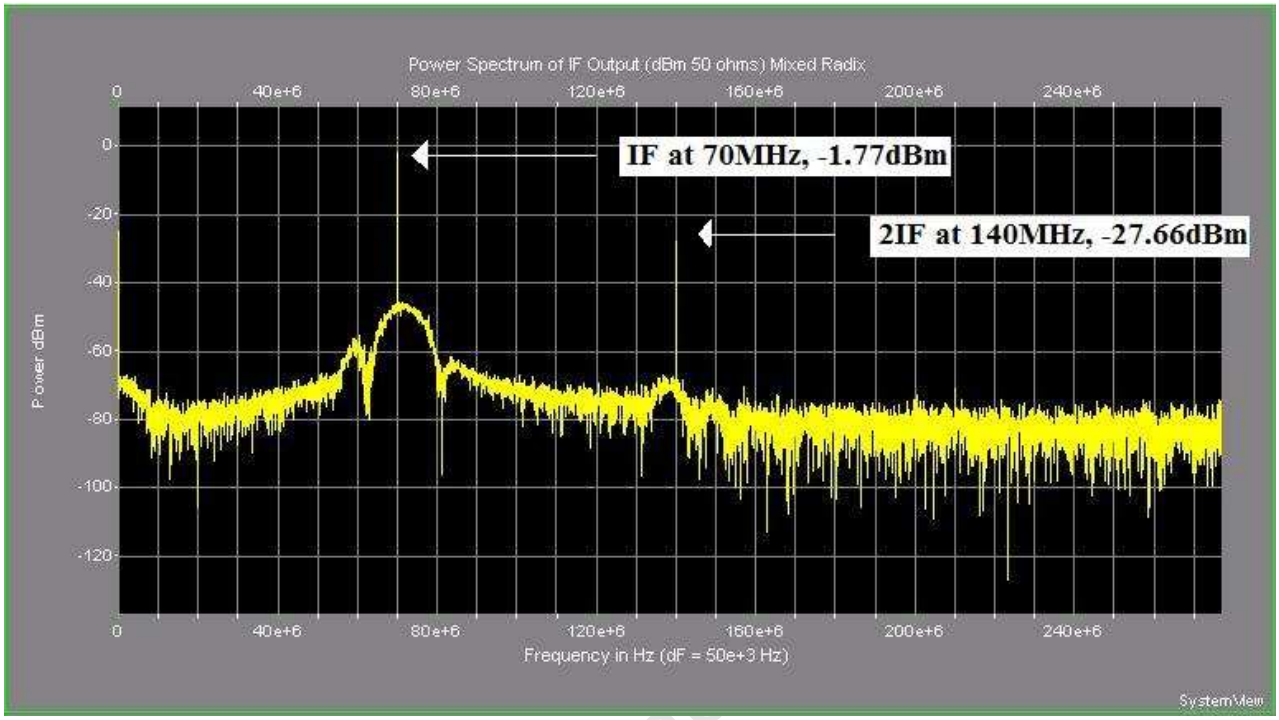

Figure 3.3: IF output of the 3x4 receiver module in SystemView with a minimum RF input power level of -64 dBm at 700 MHz.

RF input power level (dBm)	IF output power level (dBm) with RF input frequency at 700 MHz	IF output power level (dBm) with RF input frequency at 1200 MHz	IF output power level (dBm) with RF input frequency at 1700 MHz	Average receiver gain (dB)
-34	+3.1	+3.76	+2.03	+36.96
-40	0	-1.1	0	+38.90
-64	-1.77	0	-2.86	+62.46

Table 3.2: IF output power level over the RF operating frequency with input power levels of -34, -40 and -64 dBm, with variable attenuation set to 31 dBm, 6 dB and 2 dB respectively. Average receiver gain for each input power level over the RF operating frequency band varies from +36.96 dB to +62.46 dB.

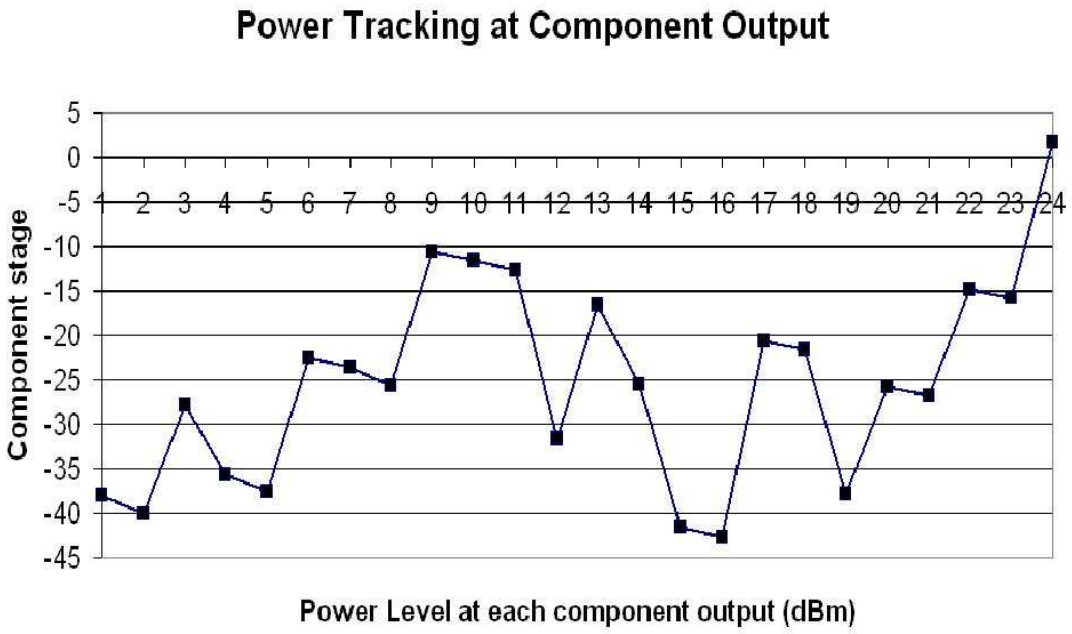

Figure 3.4: Power level tracking at each component output of the 3x4 receiver module by injecting a RF input signal at 700 MHz, with a power level of -50 dBm using SystemView.

3.2.3 Variable Attenuation

Figure 3.5 shows the IF output power level of the 3x4 receiver by varying the attenuation value ranging from 2 to 31 dB in 1 dB step. An input RF signal at 700 MHz with a power level of -40 dBm was injected into the 3x4 receiver and the IF output at 70 MHz was recorded. It is shown that the IF output power level reaches more than the expected -1 dBm due to insufficient attenuation.

3.2.4 Two-Tone Test

Harmonics, spurious reponses, and wide band noise need to be suppressed to increase the performance of the receiver [8]. Especially for a sensitive receiver, the noise level is way too high comparing to the wanted signal. In an ideal suituation, one would only want the desired IF signal at 70 MHz. But in practice, different kinds of spurious signal come into play and by predicting where it will appear, one can eliminate the occurances of the spurious signals and increase the spectral purity at IF. By performing the two-tone test, one can predict the possible frequency locations of the harmonics and intermodulation products. Definition of intermodulation products can be found in Chapter 2.

In the simulation, two-tone input frequencies at 700 MHz (f_1) and 710 MHz (f_2) are fed into the receiver (with a spacing of 10 MHz), each with equal input power level of -50 dBm. The third order intermodulation products are nearest to the fundamental frequencies (in this case, 60 MHz and 70 MHz), and are likely to fall into the desired frequency band. Therefore, observation is needed when analysing the occurrence of the

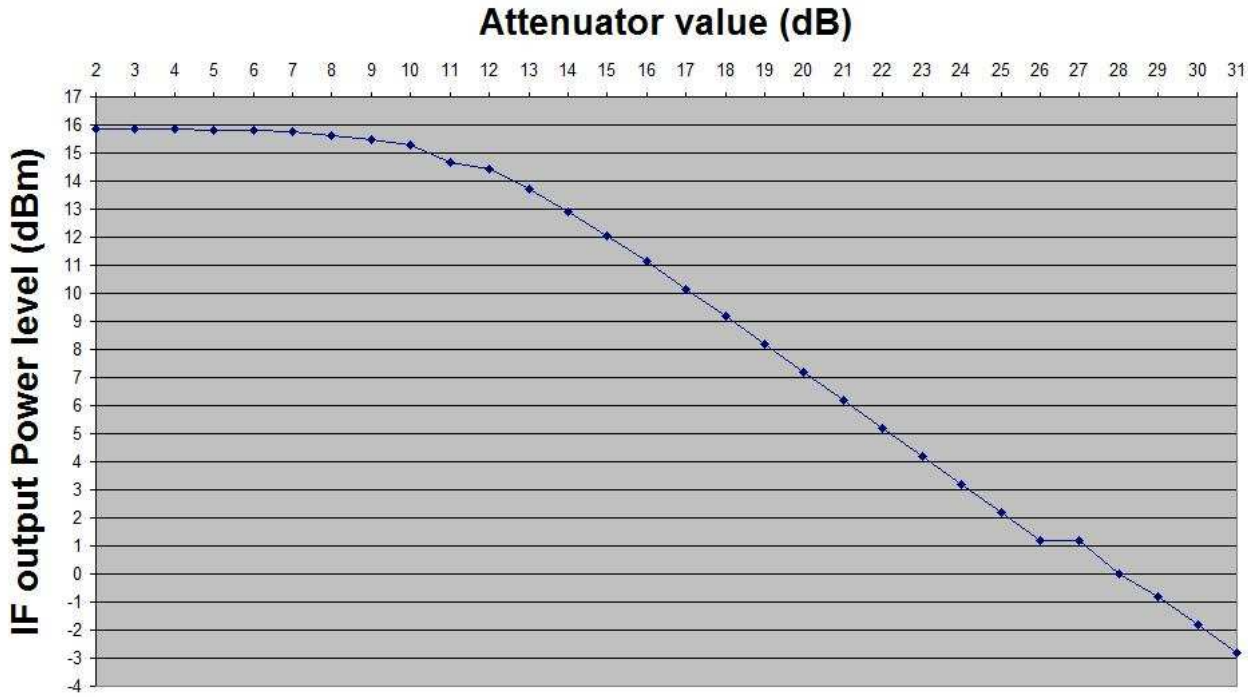

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Figure 3.5: IF output power level with an RF input signal at 700 MHz with a power level of -40 dBm. The 6-bit programmable attenuator varies from 2 dB to 31 dB in 1 dB step increment.

third order intermodulation products. Figure 3.6 shows the simulated result for the two-tone test and it shows that the power level of the third order intermodulation product at 80 MHz ($(2 \times f_1) - f_2$) is low comparing to the IF frequency at 0 dBm, and is embedded inside the system noise floor. In Chapter 5, results comparison between the simulated and measured data for two-tone test will be presented.

3.2.5 Receiver Output Noise

The internal noise generated by the 3x4 receiver can be simulated in SystemView. Figure 3.7 shows the noise generated by the 3x4 receiver module at the IF output of 70 MHz with a bandwidth of 24 MHz. From the same figure, the average noise power of the noise floor fluctuates between -100 to -80 dBm, and the internal noise generated by the 3x4 receiver module is about 20 dB as it increases the average noise floor to -60 dBm.

3.2.6 Conclusion

This chapter describes how the 3x4 receiver is simulated in the SystemView environment. Each of the components used in the 3x4 receiver is modelled in SystemView according to the specifications the manufacturer provided. The simulation results are discussed, and it is concluded that the input RF power level must be within the specified operating range (i.e. -64 to -34 dBm). Otherwise, saturations of the receiver and intermodulation products will be generated. The power tracking of each component along the 3x4 receiver module

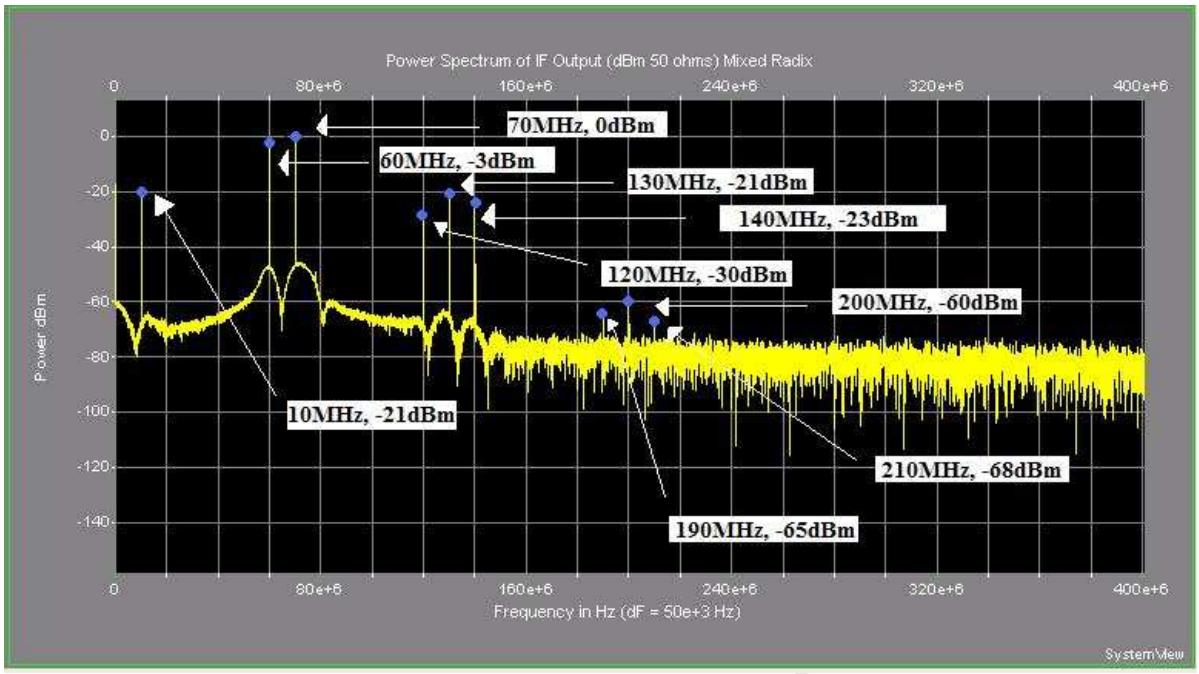

Figure 3.6: Two-tone test with frequencies at 700 MHz and 710 MHz ($f_1$and $f_2$respectively), each with an input power level of -50 dBm.

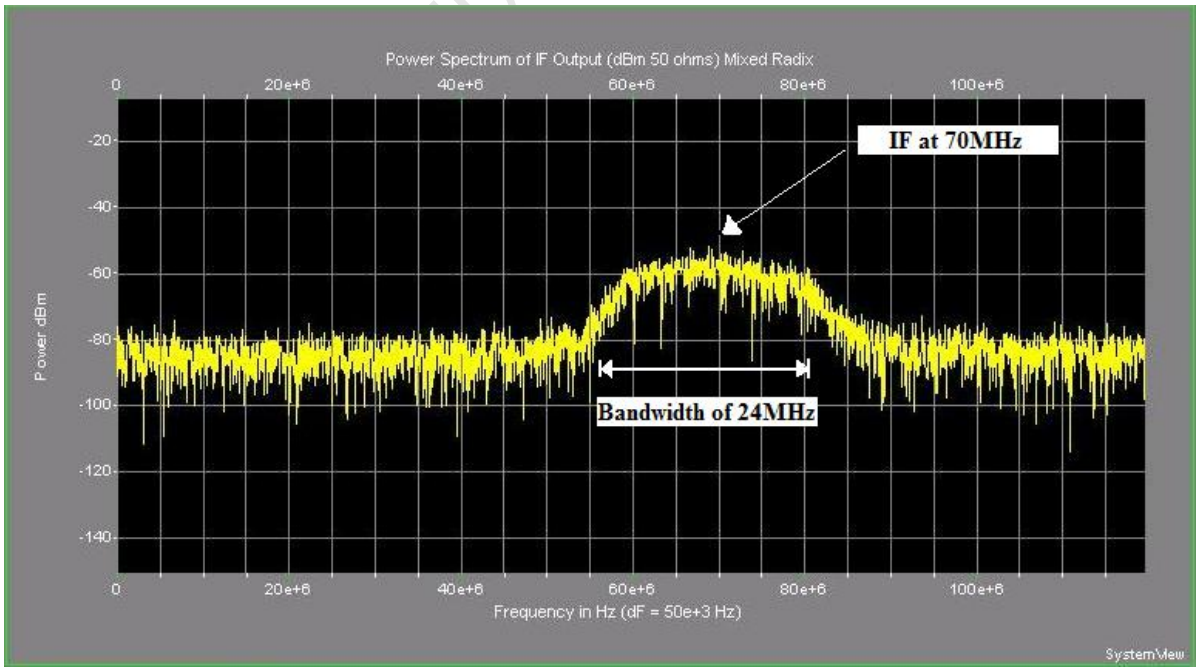

Figure 3.7: Receiver noise of the 3x4 receiver module in SystemView at IF output frequency of 70 MHz with a bandwidth of 24 MHz.

in SystemView ensured that the input power levels going into the components (especially amplifiers and mixers) did not exceed the specified power level, and hence saturate the components, resulting intermodulation products. From the two-tone test simulation result, it predicts correctly where the intermodulations would appear compared to the theory. It is concluded that the theoretical predictions agree with the simulation results obtained from SystemView. These simulation results obtained are then compared with the measured results in Chapter 5. In the next chapter, the integration of the 24-channel RF receiver rack will be discussed.

Chapter 4

24-Channel RF Receiver Rack

This chapter presents an overview of the design for the 24-channel RF receiver rack and the 25-channel calibrator integrated locally by Tellumat (Pty) Ltd. The design trade-offs together with the explanation of the functionality of the local oscillators, power supply, and rack controller are discussed first. Thereafter, the complete system block diagram of the RF rack is demonstrated, and its functional relationships with other subsystems within the RF rack are discussed. Next, the 25-channel calibrator that calibrates the receiver modules before use with the antennas, is considered. Lastly, problems encountered during the integration process are reviewed. The aim of this chapter is to give a brief review of the major subsystems of the 24-channel RF rack without going into the schematic design level.

4.1 Overview of System Architecture

As mentioned in Chapter 2, the purpose of building the 24-channel RF receiver is to perform the near field test for the 3x4 dual polarised Vivaldi antenna arrays. The twenty-four receiver modules and the two backplanes (motherboards) are existing hardware that was procured from the Australian Telescope National Facility (ATNF). In the development of the ATNF receiver rack, the two 32-way splitters built for distributing the RF LO and IF LO to the twenty-four receiver modules are included in delivery, but were not assembled as part of the RF rack. Tellumat (Pty) Ltd has designed and produced another two local oscillator synthesizer boards to replace the two 32-way splitters used by the xNTD project.

The system block diagram of the complete 24-channel receiver rack is shown in Figure 4.1, as can be seen, the RF rack consists of the following major components:

- Power Supply Unit (qty 1). This takes in an AC input power of 100-240V and provides adequate power to the other subsystems.
- Receiver Modules (qty 24). Each receiver module employs the dual-conversion superheterodyne receiver architecture, whose design was discussed in Chapter 2.

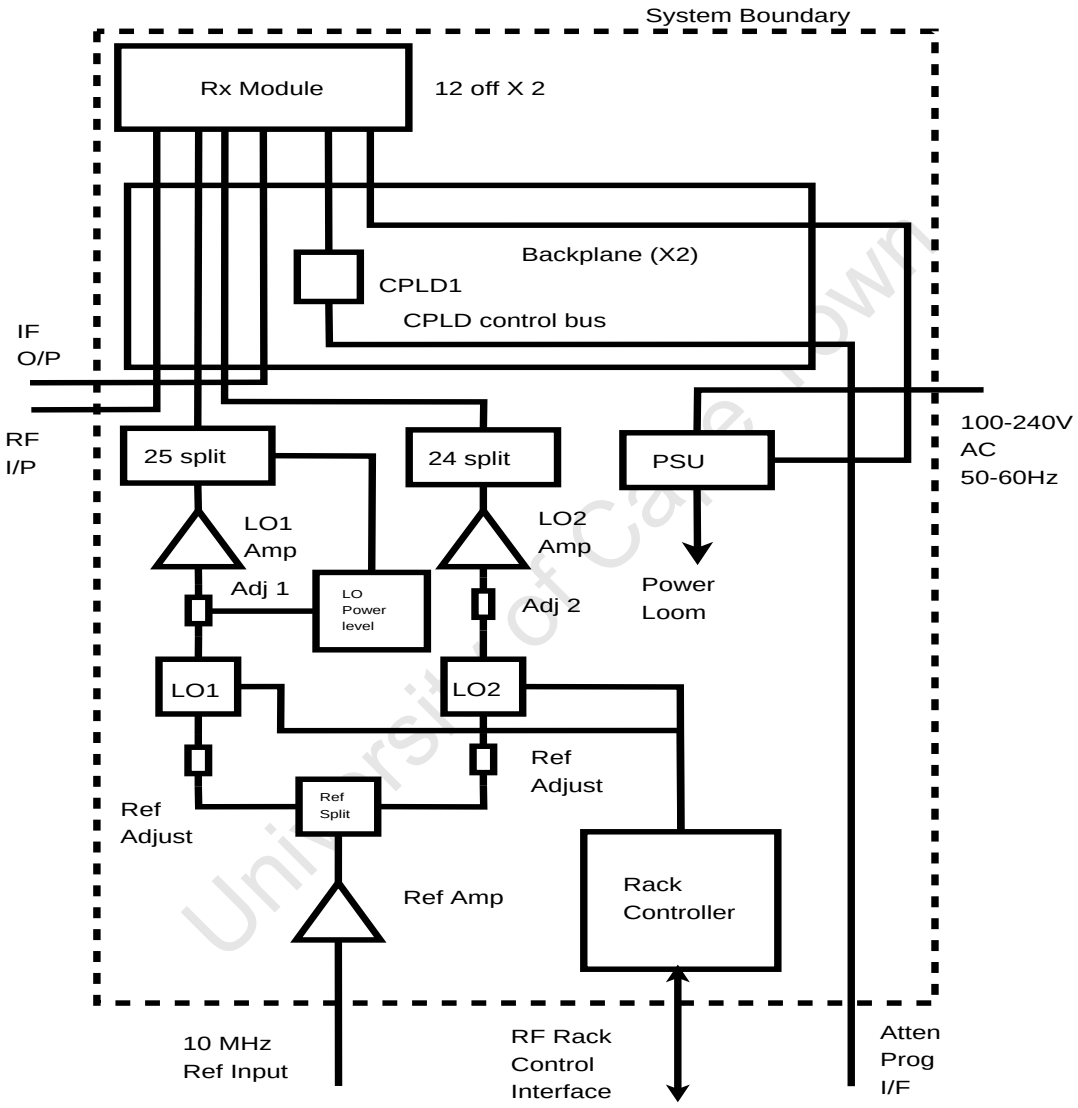

Figure 4.1: RF Rack System Block Diagram. [12]

- Rack Controller (qty 1). It consists of a microprocessor, which is responsible for programming the attenuators on the receiver modules and local oscillators frequency.
- LO1 Synthesiser (qty 1). This is tunable over the frequency range from 3.28 GHz to 4.18 GHz and the LO signal is phase synrchorised with the 10 MHz reference signal.
- LO2 Synthesiser (qty 1). This oscillator provides a fixed frequency at 2.414 GHz (or 2.554 GHz) and is phase synchronised with the 10 MHz reference signal.
- Motherboards (qty 2). Twelve receiver modules can be mounted on each motherboard.

The interfaces of the RF rack 's front panel are shown in Figure 4.2, and the connector types for each interface are listed on Table 4.1.

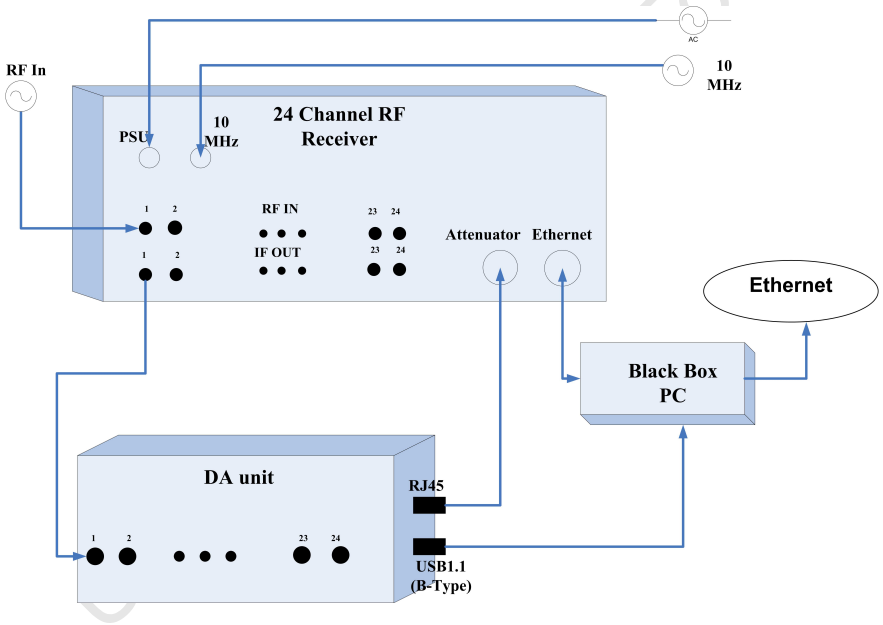

Figure 4.2: Interfaces of the RF Rack's front panel.

A number of specific requirements for the RF rack are described below:

- The RF cables and connectors are required to be durable for frequent connection and disconnection, therefore cables are shielded with protective boots to reduce electromagnetic (EMC) radiation.
- The ATNF project used a rack of size 4U; the KAT team concluded that this size was not big enough to accomodate all the subsystems while maintaining good airflow within the RF rack. Thus a rack of size 6U is used for the 24-channel RF rack [34].
- Special attention must be given to the effect of EMC radiation generated by the local oscillators, the PSU, and also the microprocessor from the rack controller.

Name	Type	Notes
RF Input	SMA Female	24 inputs, each takes in an RF input frequency from 0.7 to 1.7 GHz
IF Output	SMA Female	24 outputs, each provides an IF output frequency at 70 MHz with -1 dBm power level
10 MHz reference input	BNC	Takes in 10 MHz sinusoidal signal with a power level of 0 dBm from a measuring equipment
Main Power Input	IEC Kettle plug socket	Supplies power to the RF rack and its subsystems
RF Attenuator Programming Input	RJ45	Takes in the signal sent from DA unit to program the 6-bit programmable attenuators of the 24 receiver modules
RF Rack Control Input	RJE	Used to program the frequency of the local oscillators of all the receiver modules via an Ethernet connection

Table 4.1: Interfaces of the RF rack receiver and its corresponding connector types

For simplicity, throughout this chapter, the 24-channel receiver rack will be referred to as the RF rack.

4.1.1 Power Supply Unit (PSU)

The Power Supply Unit (PSU) used for the RF rack is a commercial off-the-shelf (COTS) component from ASTEC. The actual PSU (LPQ153C) unit is shown in Figure 4.3. It was

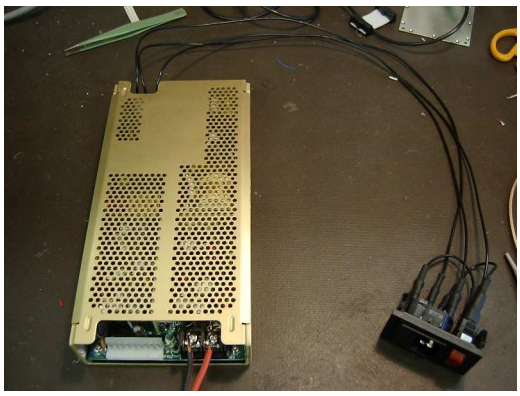

Figure 4.3: Power Supply Unit together with the IEC kettle plug used for the RF rack.

chosen because of its ability to provide low ripple output and suppress radiations from electromagnetic interference (EMI) filtering [4]. In addition, it also has a remote inhibit feature, which increases safety when the PSU needs to be shut down [1]. This PSU is a

switch-mode unit. The choice of this instead of a linear PSU, is because the 24-channel receiver rack is limited in size. Switch-mode PSU is much smaller in dimension compared to linear PSU, and also lighter in weight [21]. The role of the PSU is to provide a wide range of voltages (±15V, ±5V to +25V) to various subsystems within the RF rack. Figure 4.4 shows the power distribution from the PSU to various subsystems. The PSU draws in an AC input power from the SK4 connector as shown. Both the SK2 and SK3 connectors of the PSU are connected to the rack controller to supply the required power. The rack controller is responsible for delivering the required output voltages needed by the two motherboards, the two local oscillators, the two fans for heat dissipation, and the LED display.

The PSU supplies an input voltage of at least +5.8V to the two motherboards (on each of which are mounted 12 receiver modules) because each of the receiver modules draws a current of 0.43A. The two synthesiser boards require ±15V and +5V from the rack controller to drive the voltage regulators and amplifiers on the boards. Lastly, the PSU itself is double shielded to prevent radiation from leaking out.

4.1.2 Receiver Modules

Figure 4.5 shows one of the receiver modules built by ATNF. Each of the receiver modules has four sub-miniature B (SMB) male connectors, three inputs (RF input, RFLO and IFLO) and one IF output (IF output), which is shown in Figure 4.6. By adopting the concept of the superheterodyne receiver architecture, the first oscillator is responsible for up-converting the RF signal to 2.484 GHz and then down-converting this signal to IF at 70 MHz with a bandwidth of 24 MHz. A more in-depth discussion of the architecture and design of the receiver module can be found in Chapter 2.

4.1.3 Rack Controller

The rack controller contains a microprocessor (PIC18LF6620) and is responsible for setting the frequency of the two local oscillators. An Ethernet control interface is used to communicate with the other subsystems of the RF rack. Data is transported by means of a User Datagram Protocol (UDP) over a Category 5 (CAT5) cable. A ferrite is attached to the CAT5 cable to suppress the radiation from the Ethernet. The PSU is connected to the rack controller, which provides the following functions:

- Allows the user to choose which synthesiser boards (LO1 or LO2) are to be enabled.
- Allows the user to set the tunable frequency of the LO1 synthesiser board and the fixed frequency of LO2 synthesiser board.
- Distributes power to the fans to dissipate heat and increase airflow within the rack.

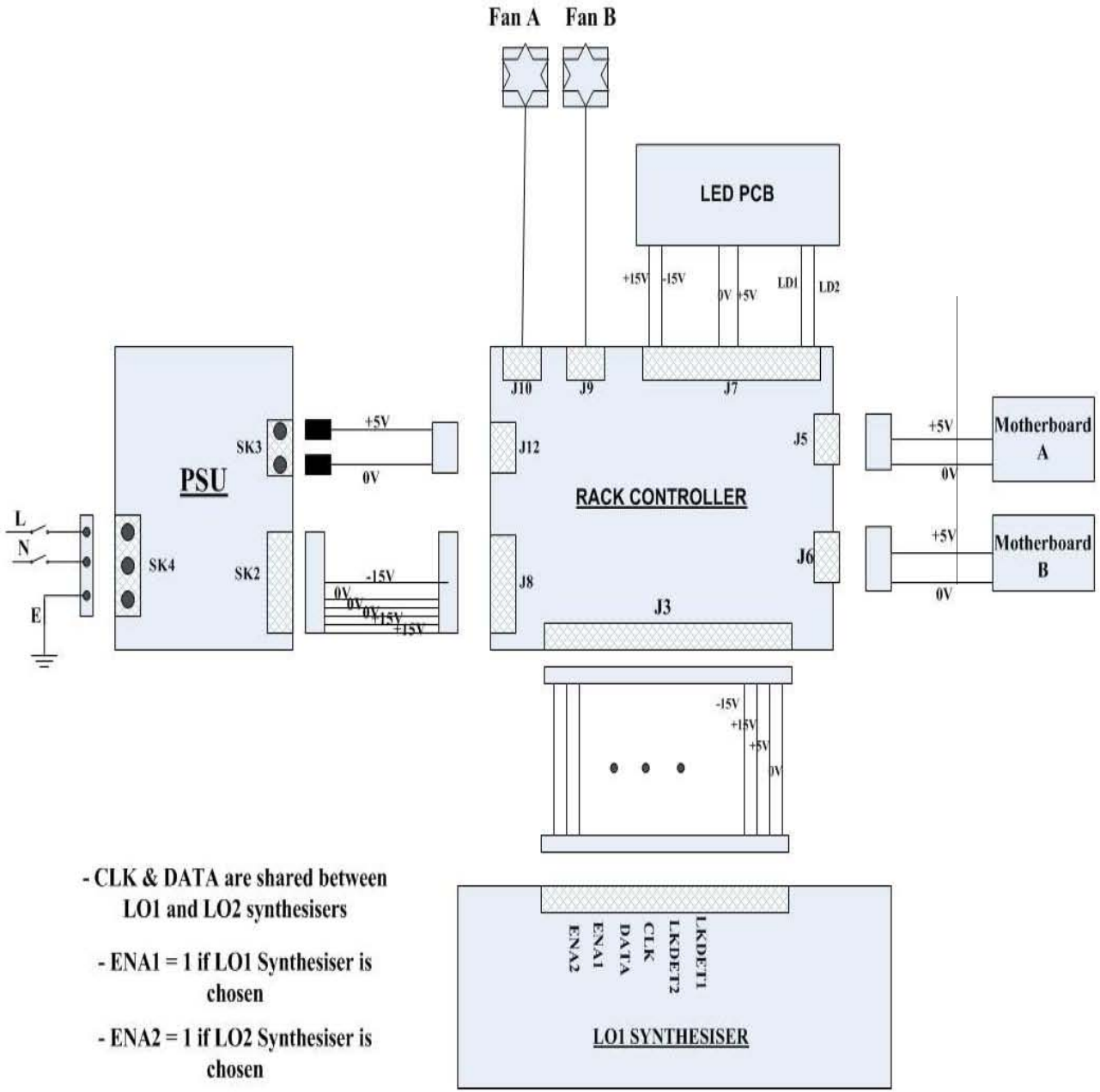

Figure 4.4: Power Distribution diagram from the PSU to the subsystems within the RF Rack.

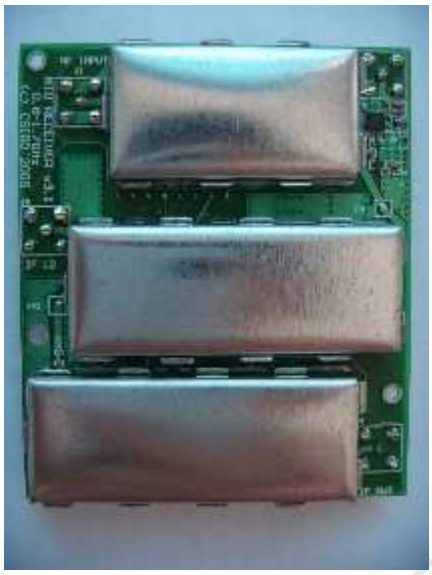

Figure 4.5: Top view of one of the receiver module with shielded covers on.

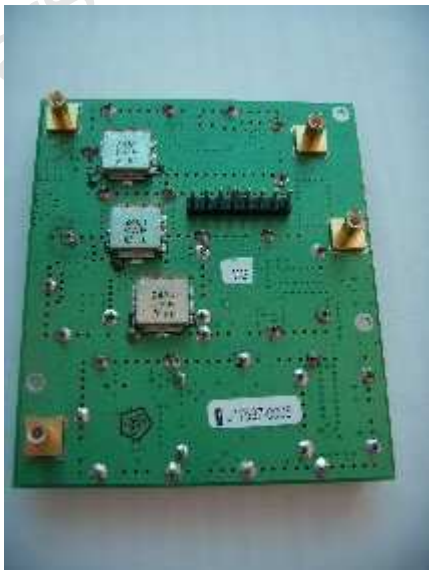

Figure 4.6: Back view of one of the receiver module. Four SMB male connectors are on each of the receiver modules.

- Indicates if the synthesiser frequencies are being logged via the RF cable and displays this on the LED display. If the frequency is logged, the LED will turn on.

In addition, there is a ribbon cable connecting the rack controller to the LO1 synthesiser board. This configuration also applies to the LO2 synthesiser board.

4.1.4 Local Oscillator Synthesiser Boards

In a superheterodyne receiver, it is important to provide a highly purified LO signal for frequency mixing. Moreover, the LO source must be able to move rapidly between frequencies in a given time [32]. In most modern receivers, synthesisers are used as the frequency source to generate all the individual frequencies over the tunable frequency band without a need for multiple oscillators [27]. For the design of the RF rack synthesiser boards, an indirect synthesis method called the phase-locked loop (PLL) is used. A +15 V input voltage from the PSU is regulated by a voltage regulator (LM2941S5) and its output is used to drive the tunable voltage-controlled oscillator (VCO). The LO2 synthesiser board uses JTOS3000 (the LO1 synthesiser board uses MW500-1451) as the VCO, which provides an accurate and precise reference frequency within the frequency range from 2.3 to 3 GHz, and its output frequency is divided by N (÷N) using a programmable divider, whereafter it is fed into the synthesiser chip (PE3240). The PE3240 consists of a 10/11 prescalar, whose output is fed to the phase detector and is compared with the reference signal. The phase detector output voltage is proportional to the difference in phase of these two inputs, and is used to align the VCO frequency [32]. Pin 2 of the PE3240 goes HIGH to indicate that the loop is locked. The output of the PE3240 first goes through a loop filter to suppress any unwanted signals, then it is fed back to the VCO to adjust its frequency until the divided frequency equals the reference frequency. The two synthesiser boards are shielded in metal cases and the printed circuit board 's (PCB) radiation is reduced by the use of gaskets on the edge of each PCB. The output of the oscillator is then amplified and distributed into 24-ways output. Figure 4.7 shows the rack controller and synthesiser board with twenty-four RF flexible cables (LMR100 with loss of 1.09 dB/m) at each output of the splitter. The splitters for the two synthesiser boards are designed at its required operating frequency using micro-stripline by Tellumat (Pty) Ltd. The design of the LO1 and LO2 synthesiser boards is discussed individually in detail in the following sections.

4.1.4.1 LO1 Synthesiser Board

The LO1 Synthesiser board is tunable over the frequency range from 3.15 to 4.2 GHz. Figure 4.8 is a simplified block diagram of the LO1 synthesiser board. The LO1 power amplifier boosts the output power of 0 dBm to the power level required (i.e. > 11 dBm) before the VCO signal is split into 32-ways by the splitter network. 24 of the splitter output ports are distributed as LO inputs to the receiver modules with a power level of

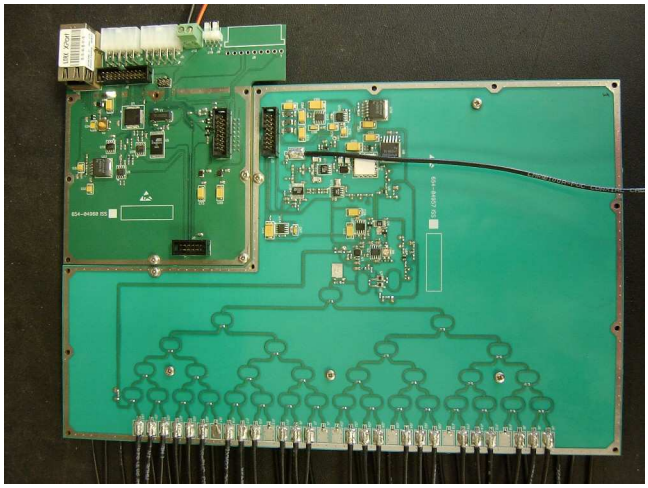

Figure 4.7: The physical integration of the rack controller, LO1 and LO2 synthesiser boards.

-1 dBm. An extra port is used for the Power Leveling Loop and the rest of the unused ports are terminated by 50 ohm loads to suppress radiation. The purpose of the power leveling loop is to avoid power starvation at the mixer input and to ensure that all the mixers of the receiver modules are optimally driven, as frequency varies between the operating range. The input signal to the power leveling loop first goes into the power detector (AD838), which converts the RF signal to a corresponding output voltage. The output voltage goes into the voltage variable attenuator (HMC346MSG), where the signal power level is adjusted according to the DC voltage. An extra amplifier (THS4031CD) is used to provide a simple single voltage attenuation for controlling the HMC346MSG.

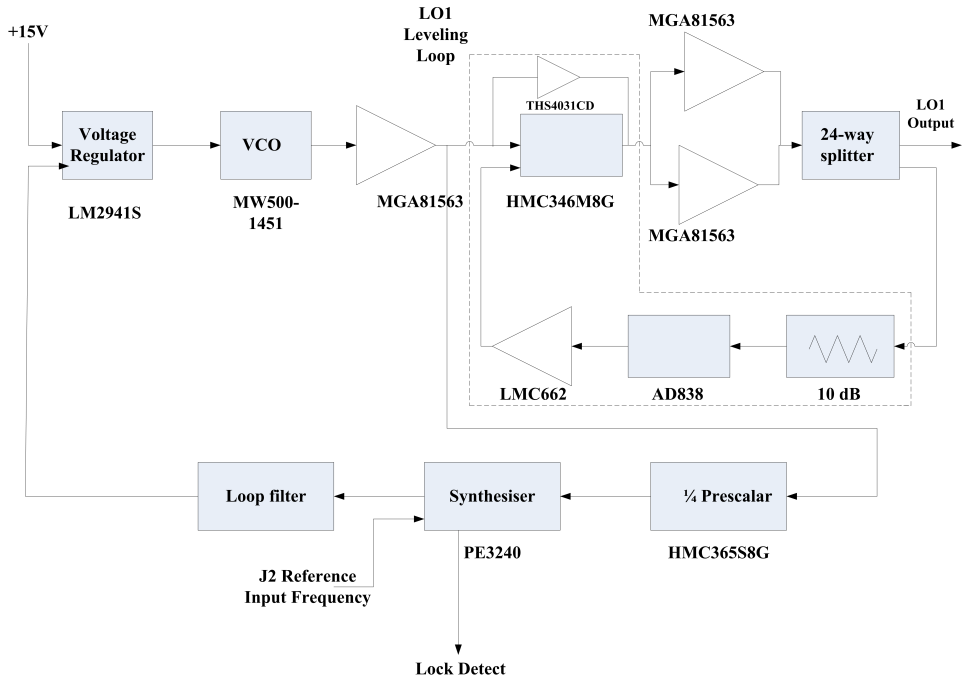

Figure 4.8: Block Diagram of the LO1 Synthesiser Board.

4.1.4.2 LO2 Synthesiser Board

The LO2 Synthesiser board provides a fixed frequency at 2.414 GHz (or 2.554 GHz). A block diagram of the major components used for the LO2 is given in Figure 4.9. The general design concept of the LO2 synthesiser board is similar to that of the LO1 synthesiser board, except that it does not need the power leveling loop, as its oscillator frequency is fixed. An output power level at each of the splitter ports of -1 dBm is achieved.

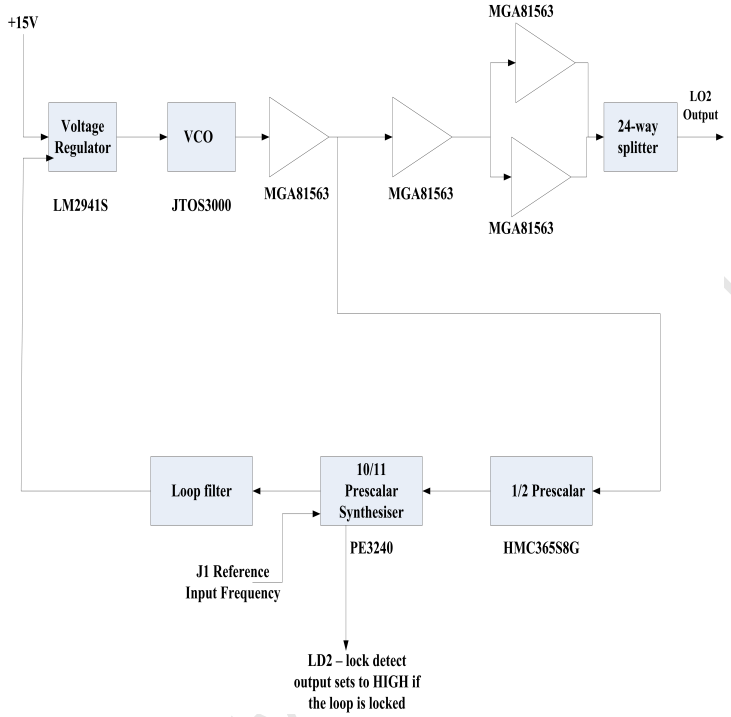

Figure 4.9: Block Diagram of LO2 Synthesiser board.

4.1.5 Motherboards

The RF rack has two motherboards, each of which can house twelve receiver modules, as shown in Figure 4.10. The motherboards handle the routing of the signals (RF inputs, IF outputs and the two LO inputs) from the receiver modules to the front-panel of the RF rack. Each channel on the motherboard consists of a Complex Programmable Logic Device (CPLD), which stores and controls the programming of the IF attenuator via the 5-bit control line. The positions of each receiver module on the motherboards is logged, and their addresses are programmed into the CPLD. A +5V input voltage is supplied from the PSU to the motherboards in order to provide sufficient current (i.e. 0.43A) to each of the receiver modules.

4.1.6 25-Channel System Calibrator

The 25-channel calibrator is required to provide 25 simultaneous calibrated signals to the 24-channel receiver. The DA unit calculates the amplitude and phase of the RF signals

Figure 4.10: Motherboard without mounting the receiver modules.

presented at the IF of 70 MHz. The obtained amplitude and phase readings of the calibrator are then used to calibrate the RF rack receiver across the whole frequency band. Figure 4.11 is a simplified layout diagram of the 25-way splitter network. The 25-way splitter network comprises twenty-seven 2-way power splitter units (ADP-2-20), each with an insertion loss of 0.7 dB, which gives a total insertion loss of approximately 18.6 dB. The operating frequency for this splitter is from 20 to 2000 MHz. The input power level to the calibrator is approximately +11 dBm and results in an output power level of -5 dBm. As the receiver only has 24 channels, the extra unused port is terminated by a 50 ohm load. It is assumed that each port of the calibrator has nominally the same output power level with respect to its phase and amplitude to the input signal.

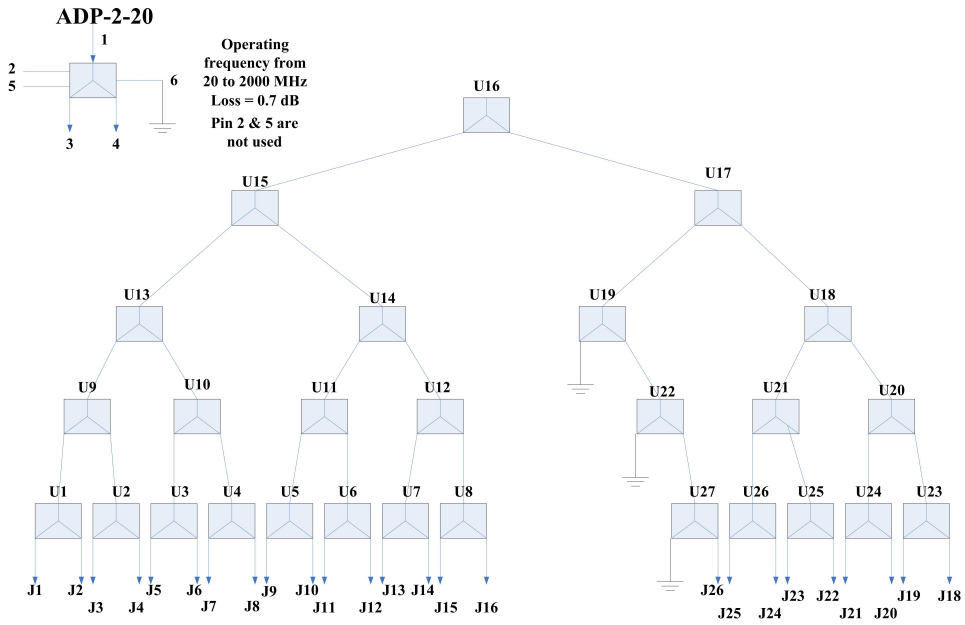

Figure 4.11: 25-way splitter calibrator layout with the unused port terminated.

4.1.7 Construction of the RF Rack

All the hardware is enclosed in a 19” high quality rack as shown in Figure 4.12, which is designed in a way to minimise EMC problems. The LO1 synthesiser board is placed

back-to-back against the LO2 synthesiser board, and both are enclosed in a metal case to prevent radiation leakage. This unit is then sandwiched in between the two motherboards.

Figure 4.12: The 19" RF rack accommodates all the hardware of the 24-channel RF receiver. The top and bottom level are for the two motherboards, with the two synthesiser boards sandwhiched in between them.

4.1.8 Conclusion

In this chapter, an overview of the design for the 24-channel RF receiver rack and the 25-channel Calibrator integrated locally by Tellumat (Pty) Ltd is presented. Problems encountered during the integration were reviewed. It has shown that all the sub-components are successfully being integrated into the 19" rack. In the following chapter, the acceptance tests conducted for all the major subsystems of the RF rack are presented. The purpose of each test is described, and the results obtained are analysed.

Chapter 5

Acceptance Test Procedures and Results Comparison

The performance of the integrated 24-channel RF receiver rack can be evaluated by conducting acceptance tests. This chapter details the acceptance tests of the RF receiver rack carried out by the client (KAT). The acceptance tests procedures, together with the measurement results carried out by the contractor (Tellumat (Pty) Ltd) can be found in Appendix A. The contractor was provided with twenty-four built and tested receiver modules and two motherboards by the customer. The responsibility of the contractor is to develop the two local oscillators discussed in section 4.1.4 and integrate the subsystems into the RF receiver rack. For the sake of completeness of this dissertation, full functional tests of the RF receiver rack were carried out at the University of Cape Town (UCT) by the client. Lastly, results obtained from the simulations (as described in Chapter 3) using SystemView are compared with the measured results from the acceptance tests and are presented in this chapter.

5.1 Client ATPs

Table 5.1 lists the laboratory tests conducted by the contractor and client. The 24-channel RF receiver under test was considered as a black box with RF signal as input and the twenty-four IF signals as outputs. The acceptance tests that discuss in this chapter only examines the performance of the 24-channel RF receiver rack and excluding the actual field test with the dual-polarised Vivaldi antennas discussed in Chapter 2. For further test procedures and results for the field test, reader should refer to [30].

5.1.1 Preliminary Considerations in Receiver Test

The 24-channel RF receiver can receive RF signal with a single-signal dynamic range of 30 dB (from -64 to -34 dBm) with a frequency range from 700 MHz to 1700 MHz. The

	Contractor	Client
1. LO1 Synthesiser Board	a. Output power level at the LO1 24-way splitter	-
	b. Amplitude for each output channels	-
	c. LO1 is tunable within its specified frequency range	-
2. LO2 Synthesiser Board	a. Output power level at the LO2 24-way splitter	-
	b. Amplitude for each output channels	-
	c. LO2 provides a fixed frequency at 2.414 GHz	-
3. PSU	a. Appropriate voltages are distributed to all the subsystems	-
4. Motherboards	a. Output voltages are correctly distributed to each ports	-
5. RF Rack	a. IF frequency response occurs at 70 MHz	a. Single signal test
		b. Two-signal test

Table 5.1: Acceptance Tests Allocation for the RF rack.

type of input signals being apply to the receiver under test can characterise the performance of the receiver. It can be categorised into two conditions, namely

- Single-signal test
- Two-signal test (also known as two-tone test)

More details on each test is discussed and results comparison will also be presented in the following sections.

5.1.2 Channel Isolation

The channel gain for each of the IF port of the receiver under test can be measured by connecting each channel port to the power meter. The output power level for all the twenty-four IF output ports of the receiver are expected to have the same amplitude, and thus, having the same channel gain. The power level for each port can be measured by varying the power level of the RF input signal applied to the receiver under test between the specified operating power level of -64 dBm to -34 dBm. The frequency response for all twenty-four output ports of the receiver was measured using a spectrum analyser [1] and the IF output of the receiver is expected to have a centre frequency at 70 MHz with a bandwidth of 24 MHz. The test setup for measuring the receiver output power level and frequency response is shown in Figure 5.1.

[1] Spectrum Analyser Model E4407B was used for measurement.

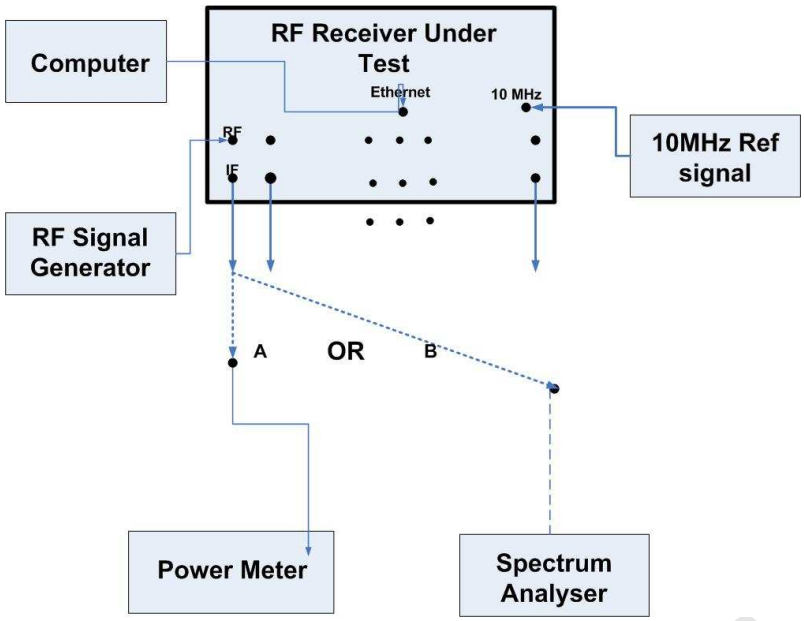

Figure 5.1: Test setup for measuring the output power level and frequency response of all the twenty-four outputs of the receiver under test.

The channel gain for each of the twenty-four channel at various RF input frequency (700 MHz, 1200 MHz and 1700 MHz) with input power level of -50 dBm, and attenuation set to 18 dB is shown in Figure 5.2. It appears that at high RF input frequency (i.e. 1700 MHz), the channel gain has a trend to be higher (maximum of -0.56 dB for port 1 and minimum of -2.87 dB for port 24) comparing that at low RF input frequency (i.e. 700 MHz). The maximum and minimum balance between channels over the operating RF input frequency band is shown in Table 5.2. Unfortunately, SystemView cannot simulate channel isolation and thus no results can be compared, but Table 5.3 compared the simulated IF output power level for any given channels to the averaged measured IF output power level. The measured IF output power levels over the RF input frequency band are lower than the simulated result. This is because the simulated results did not take into account of the possible losses caused by the physical integration of the RF rack.

RF input frequency	Maximum channel balance (dB)	Minimum channel balance (dB)
700 MHz	1.7 (between port J12 and J16)	0.2
1200 MHz	1.4 (between port J13, and J23)	0.3
1700 MHz	1.4 (between port J2, and J24)	0.3

Table 5.2: Maximum and minimum channel balance over the RF input frequency band (i.e. 700 to 1700 MHz), with input power level at -50 dBm.

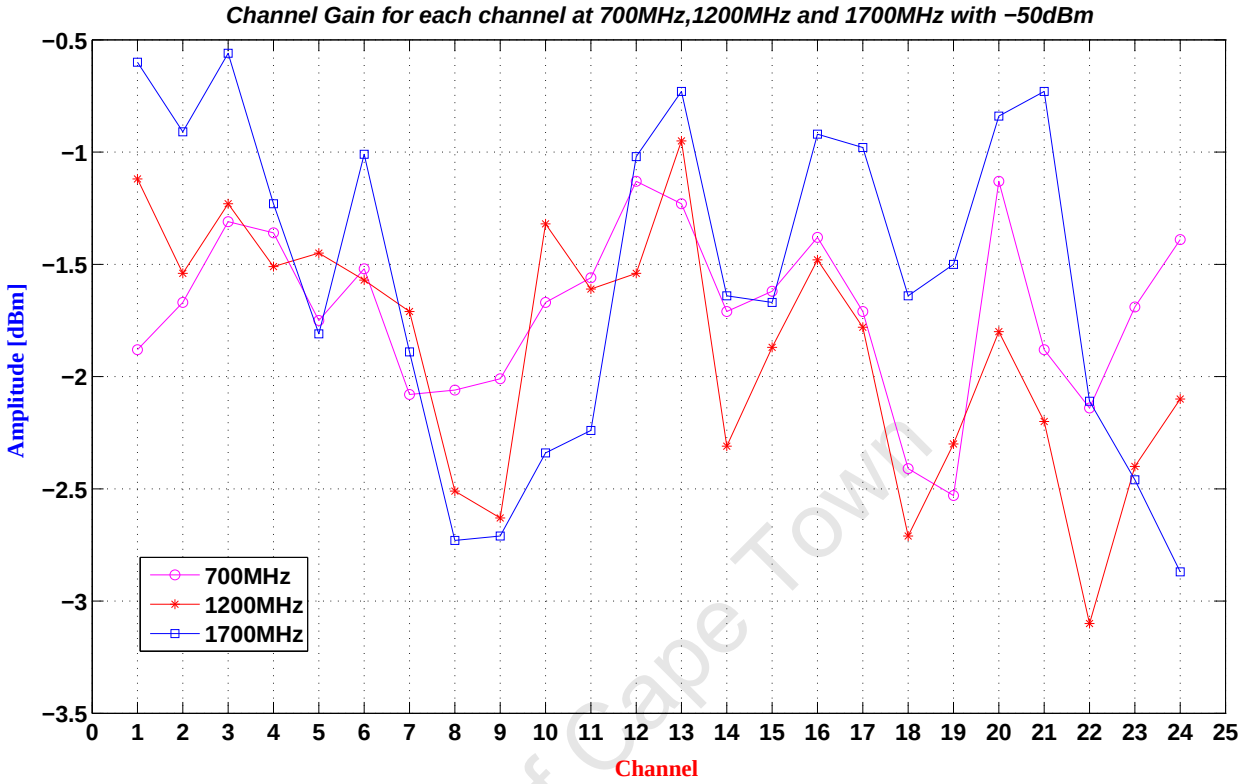

Figure 5.2: IF output power level in dBm for twenty-four channels with RF input power level at -50 dBm. The test was done at 700 MHz, 1200 MHz and 1700 MHz. It is shown from the plot that the IF output power level at the higher frequency range (i.e. 1700 MHz) has a trend to fluctuate more comparing with the lower frequency (i.e. 700 MHz).

RF input frequency	Simulated IF power level (dBm)	Measured IF power level (dBm)
700 MHz	+1.78	-1.7
1200 MHz	+0.93	-1.9
1700 MHz	-0.86	-1.5

Table 5.3: Result comparison of the IF output power level from simulation and measurement.

5.1.3 Operating Dynamic Range

In order to test that the 24-channel RF receiver is capable to receive an RF input signal at the specified operating frequency range from 700 MHz to 1700 MHz, the output power level of -1 dBm is needed to be achieved at the IF output so that it can be fed into the DA unit for signal processing. By varying the RF input power level from -64 dBm to -34 dBm within the operating frequency range, the IF output power level is measured by using a spectrum analyser. The 6-bit programmable attenuator is required to be programmed appropriately by the external computer interface to provide an output power of -1 dBm. The higher the input RF power level, the higher the attenuation value needed be set. The laboratory setup for this test is the same as Figure 5.1. Figure 5.3 shows the measured IF output power level by varying the RF input power level within the operating frequency range. It is shown from the result that the desired IF output power level of approximately -1 dBm was achieved with varying RF input power level from -64 dBm to -34 dBm. Any other RF input power that is not within this range will not reach the required -1 dBm IF power output. Figure 5.4 shows the simulated results with an IF output power level over the RF passband operating frequency. Comparing this with the measured results, with an RF input power of -70 dBm, the simulated result shows that the IF output power is about 4 dBm less than the measured value, and with an input RF power of -34 dBm, the simulated result is 4 dBm higher than the measured IF output power level.

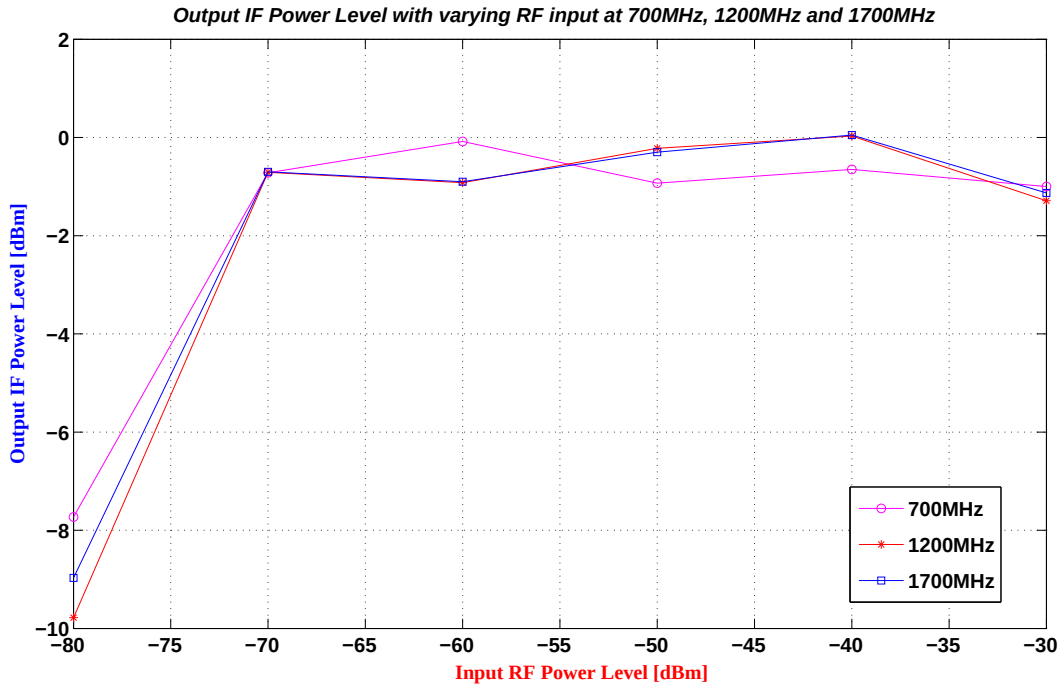

Figure 5.3: IF output power level measured in dBm with an input RF operating frequency of 700 MHz, 1200 MHz and 1700 MHz with varying input power level.

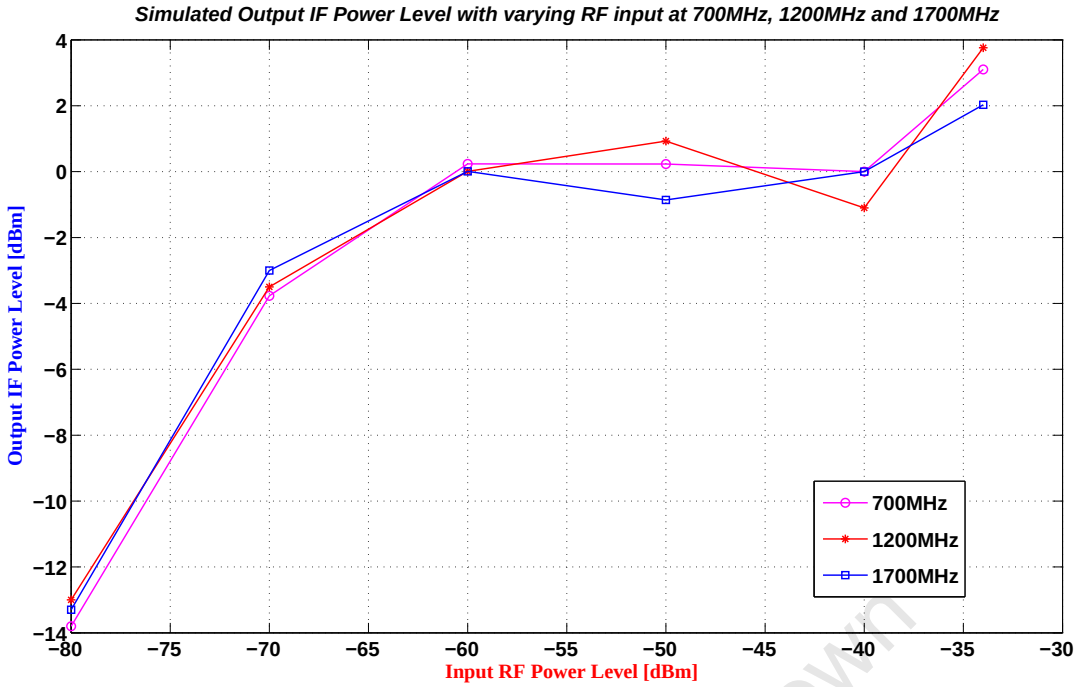

Figure 5.4: IF output power level simulated in dBm with an input RF operating frequency of 700, 1200, and 1700 MHz with varying input power level.

5.1.4 Channel Intermodulation Distortion

The purpose of the two-tone test is to determine how well the receiver performs when separating two signals that are a few MHz apart in frequency. In order to ensure the appearance of the third-order intercept and intermodulation to occur, the amplitude of the two signals needs to be adjusted to a level that is high enough to saturate the receiver and results in intermodulations. More explanation on the concept of spurious signals generated when performing two-tone test is explained in Chapter 3. The laboratory test setup for the two-tone test is shown in Figure 5.5. In this figure, there are two input signals, namely, $f_1$and f_2 with the same amplitude that are generated by two sweep oscillators [2]. These signals are closely spaced in frequency (i.e. 10 MHz apart for this test). Two signal generators were set to 10 MHz spacing apart, and these two signals are coupled by the 25-way calibrator discussed in Section 4.1.6 and fed into the RF receiver rack. The input RF signal level varies at bottom, middle and top receiver band of operation (i.e. 700 MHz, 1200 MHz and 1700 MHz). The in band and out of band intermodulation products were observed at the output of the receiver rack by using a spectrum analyser. The frequency position and the amplitude (in dBm) of the in band and out of band intermodulation signals were measured and recorded.

In Figure 5.6, the in band and out of band intermodulation products with the two-tone input signal at 700 MHz and 710 MHz with a power input level of -50 dBm is shown. Table 5.4 shows how these intermodulation products were produced. The result has shown

[2]Sweep Oscillator Model - HP8350B was used for this measurement.

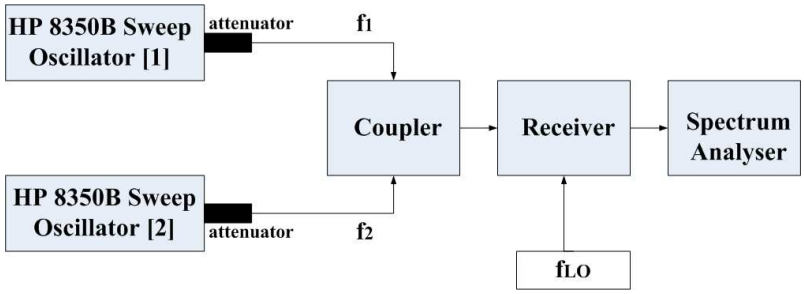

Figure 5.5: Two-tone test setup with input frequencies at $f_1$and f_2. The amplitude of both input signals are the same and by coupling the two signals using a coupler with known loss. The two-tone signal is then fed into the receiver under test and its output is read off from the spectrum analyser.

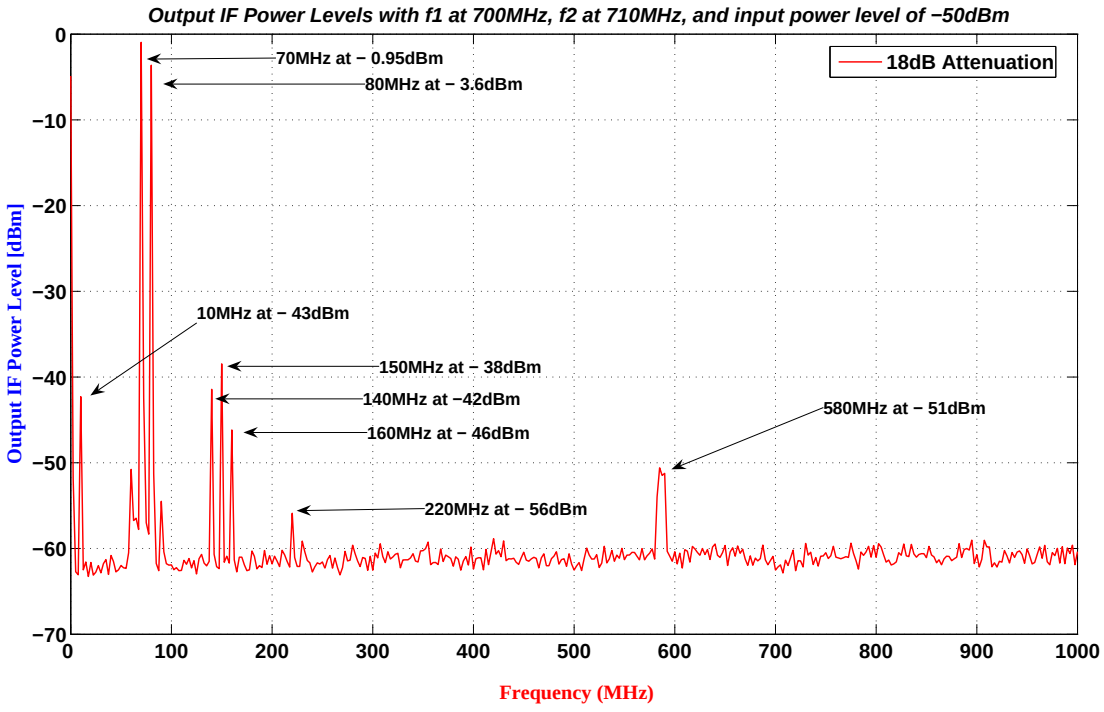

Figure 5.6: Two-tone test with frequencies first frequency at 700 MHz and second frequency at 710 MHz, each with an input power level of -50 dBm. The output of the receiver occurs at 70 MHz and 80 MHz, which corresponds to the two input frequencies with a power level close to 0 dBm.

that, an unexpected unwanted signal at 580 MHz was found. In order to investigate the appearance of the spurious signal at 580 MHz, a frequency sweep at the output of the receiver with no RF input into the receiver from 0 MHz to 2 GHz was conducted. Figure 5.7 shows the result and at 580 MHz, a signal with a power level of -75 dBm was found. This signal appeared in a regular time basis (from 08:00 to 17:00) during the day. One of the possible causes of this is the TV signal which got picked up by the sensitive RF receiver. Another unwanted spurious signal was found at 1.7 GHz with a power level of -58 dBm as shown in Figure 5.7. This signal do not vary as time goes and can be concluded that it is generated by the GSM network from the cellphone tower. These RF interferences were taken into account when analysing the result of the two-tone tests. It is to note that all the measurements were done with the IFLO frequency set to 2554 MHz (instead of 2414 MHz) to avoid unwanted spurious signals (refer to 5.1.7 for details).

Frequency (MHz)	Intermodulation Product
10	$f_1 - f_2$
70	f_1
80	f_2
140	$2 \times f_1$
150	$(2 \times f_2)$ - $(f_1 - f_2)$
160	$2 \times f_2$
580	TV signal

Table 5.4: Intermodulation products measured from the two-tone test with the first input frequency at 700 MHz and the second input frequency at 710 MHz.

Figure 5.8 shows the result comparison of the two-tone test from simulation and measurements. The frequency location of all the intermodulation products and harmonics as listed in Table 5.4 were correctly predicted by the simulation. The IF output power level for the fundamental frequencies (i.e. 70 and 80 MHz) were correctly predicted, except the other harmonics and intermodulation products power levels were about 20 dB lower than what the simulated result shows. The possible reason for this is that the model of the bandpass filters in SystemView did not characterise the realistic behaviour correctly. From the same figure, it shows that the noise floor of the receiver from the simulation is about 20 dB lower than that of the measurements. In the simulation, SystemView did not predict the internal noise generated by the testing equipment (in this case, the spectrum analyser). This 20 dB power level discrepancy can be caused by the fact that the spectrum analyser has reached its own noise floor and in the simulation, this could not be simulated. Since spectrum analysers are heterodyne receivers, the noise floor of the spectrum analyser can be reduced by reducing the resolution bandwidth. The noise spectral density ($P_{dBm/Hz}$) in dBm/Hz of the RF rack can be related with the noise power of the receiver and receiver bandwidth by using equation 5.1.1 [31],

$$P_{dBm} = P_{dBm/Hz} + 10log(BW) \tag{5.1.1}$$

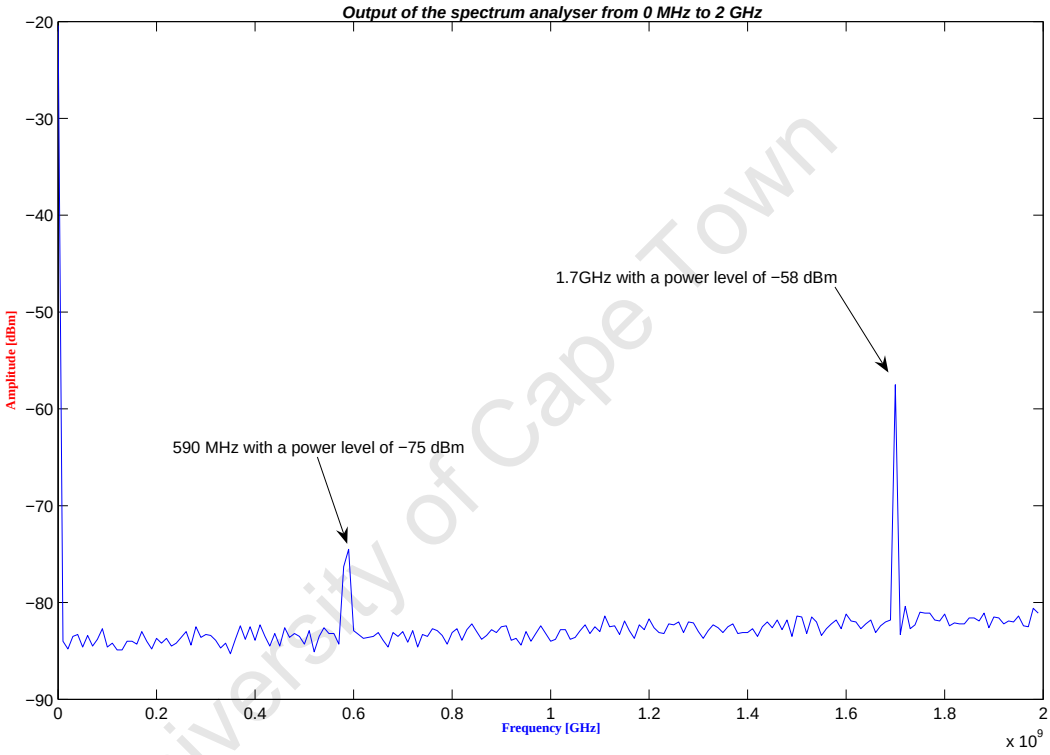

Figure 5.7: Frequency sweep from 0 Hz to 2 GHz using a spectrum analyser was conducted to investigate on the interference sources appeared in the test environment. Two unwanted interference at 590 MHz and 1.7 GHz were found to be the bi-static TV signal and GSM signal from the cellphone tower respectively. These interferences could be eliminated if the test was to perform in a RFI environment.

where P_{dBm} is the noise power in dBm, and BW is the bandwidth of the receiver in Hz. From the measurement, the spectrum analyser is set to have a resolution bandwidth of 100 kHz, and resulting a spectral noise density of the RF receiver rack of -110 dBm/Hz. If the resolution bandwidth of the spectrum analyser has to increase to 1 kHz, the output noise floor of the RF rack from the spectrum analyser will be at -80 dBm instead of -60 dBm which matches the simulated result noise floor. It is to conclude that a higher resolution bandwidth is required to be set in the spectrum analyser for measurements.

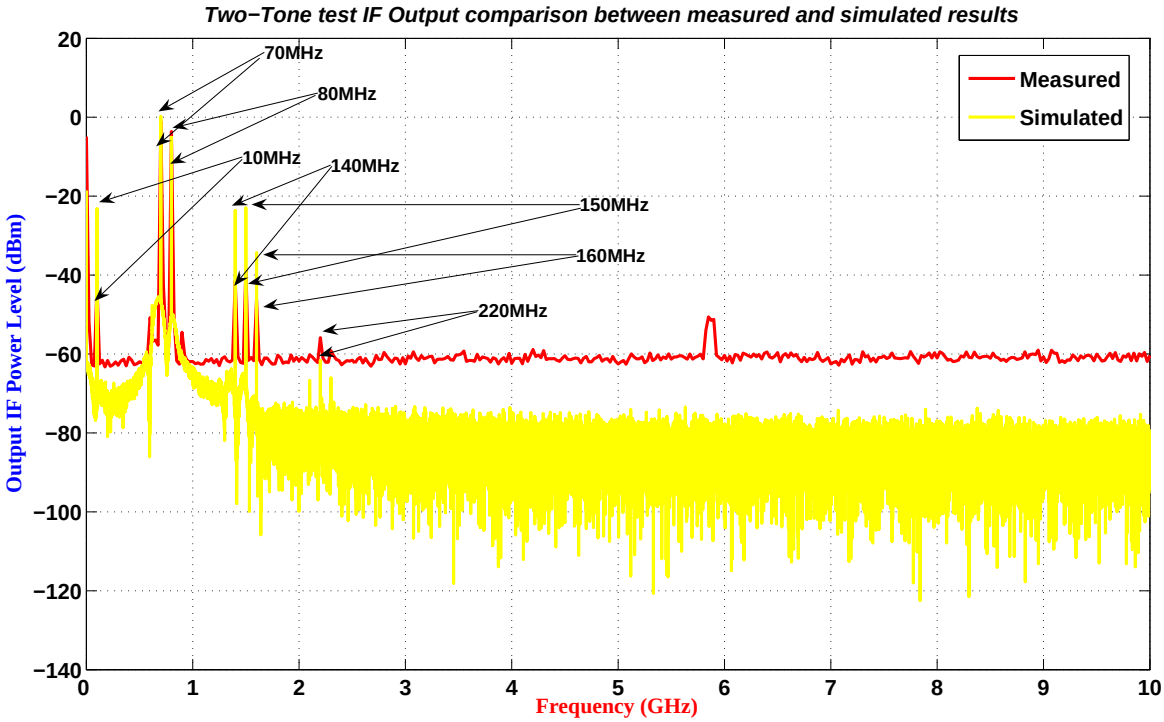

Figure 5.8: Two-tone test result comparison between simulation and measurments, with the first input frequency at 700 MHz and the second frequency at 710 MHz. Each tone has an input power level of -50 dBm.

5.1.5 Channel Gain Control

The objective of this test is to measure the channel gain of the twenty-four ports of the receiver by programming the attenuation of the 6-bit programmable attenuator from 2 to 31 dB in 1 dB step through an external computer interface. It is expected that the IF output for all the twenty-four channels are nominally the same in amplitude, given that the RF input frequency, input power level, and 6-bit attenuator value are set to the same condition for all channels. The test setup for the channel gain is the same as the frequency response test as shown in Figure 5.1. The RF input signal is tested in bottom, middle, and upper frequency (700 MHz, 1200 MHz and 1700 MHz) with a power level of -40 dBm. Figure 5.9 shows that the same IF output power level was achieved for all twenty-four channels by feeding a RF input at 700 MHz, 1200 MHz and 1700 MHz with a power

level of -40 dBm. It can be concluded that with an input RF frequency sweeping from 700 MHz to 1700 MHz, the output power level for all the twenty-four IF channels stays nominally the same without serious fluctuation as the frequency increases. And hence the rack controller interface does respond correctly to the external computer to all control commands.

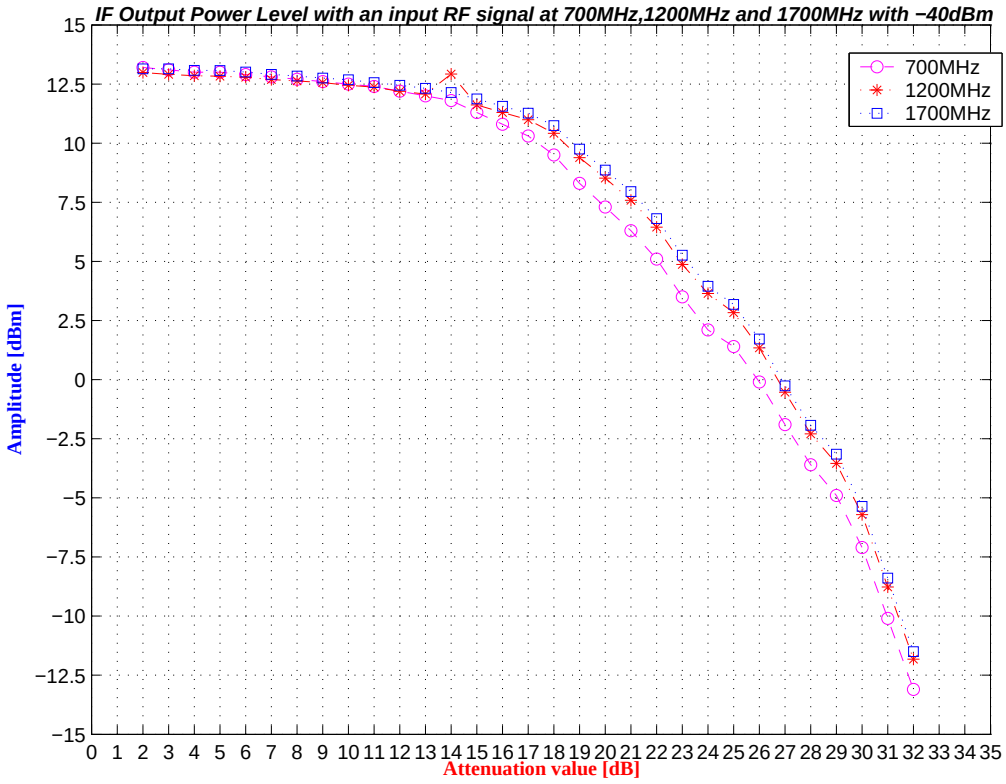

Figure 5.9: The averaged IF output power level for all twenty-four channels are plotted against the 6-bit programmable attenuation value. An RF input at 700 MHz, 1200 MHz and 1700 MHz with a power level of -40 dBm were plotted in this graph.

Figure 5.10 shows the comparison between the measured and simulated IF output power level by varying the 6-bit attenuation in 1 dB step. From the figure, it shows that the measured IF output power level drops by more than the expected 1 dBm (as the attenuation increments by 1 dB step) when the attenuation value is set to higher than 28 dB. But the simulation result did not predict this. As the IF output power level is close to the noise floor of the receiver. Thus the IF output power gets embedded into the noise floor of the receiver and is not dominating.

5.1.6 Channel Frequency Response

The internal noise generated by the 24-Channel RF receiver rack had been recorded using a spectrum analyser at the output of the receiver at 70 MHz with a bandwidth of 24 MHz. It is to note that the 6-bit programmable attenuator has not been set while this test was being conducted. Thus the 6-bit programmable attenuator only has an attenuation value of 2 dB. Figure 5.11 shows the measured average noise power of the noise floor is between

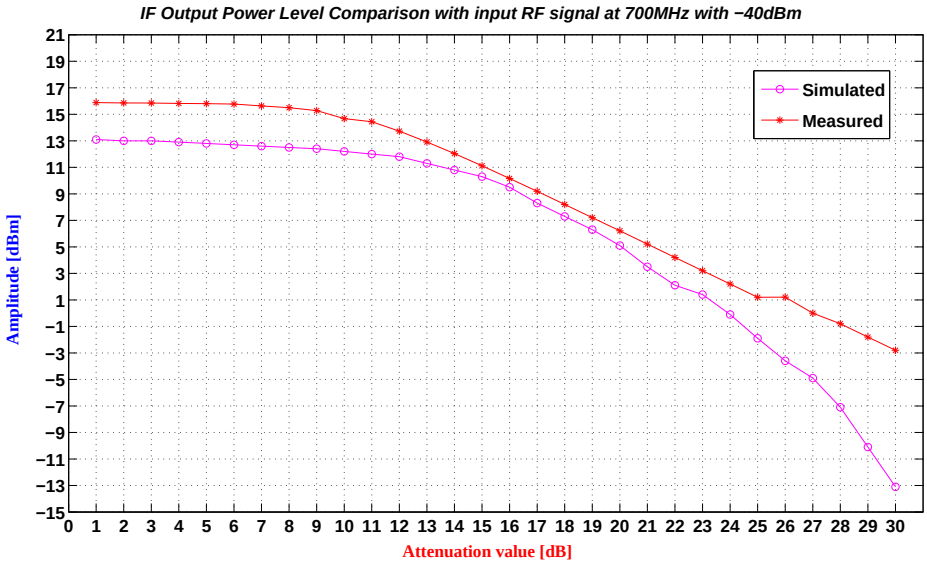

Figure 5.10: Results comparison of simulated and measured IF output power level (dBm) with varying 6-bit attenuation value from 2 to 31 dB in 1 dB step.

-80 to -70 dBm, with the simulated noise power between -90 to -80 dBm. Thus the measured noise power is about 10 dB higher than the simulated result. This means that the actual RF receiver generates more noise than the predicted. Without any RF input being injected to the RF receiver rack, the measured IF output power level at 70 MHz with a bandwidth of 24 MHz is -50 dBm. Therefore the internal noise power level of the receiver is 20 dB which increases the noise floor from -70 dBm to -50 dBm.

5.1.7 Local Oscillator Radiation

Interference products were found during the acceptance tests and the tests were re-conducted in a shielded room (RFI free environment) and spurious signals still ocurred. By connecting the spectrum analyser to the IF output port of the RF receiver rack, a signal was swept at 5 MHz steps with varying start and stop frequency as shown in Table 5.5. Later then it was found out that the spurious signals were caused by the intermodulation products between the two synthesiser boards. The problem was resolved when the LO2 frequency is set to 2554 MHz (i.e. $(2 \times 70 + 2414)$ MHz) instead of 2414 MHz.

5.1.8 Limitations for measurements

Difficulties encountered during the procedure tests due to the limitation of testing equipments provided at UCT. Therefore the channel noise factor test was not performed as there is no equipment available for it. It is suggested that a noise figure measuring equipment is needed for measuring the channel noise factor of the receiver. Another possible way for measuring the noise figure of the receiver is to perform the Y-factor test. By plunging the

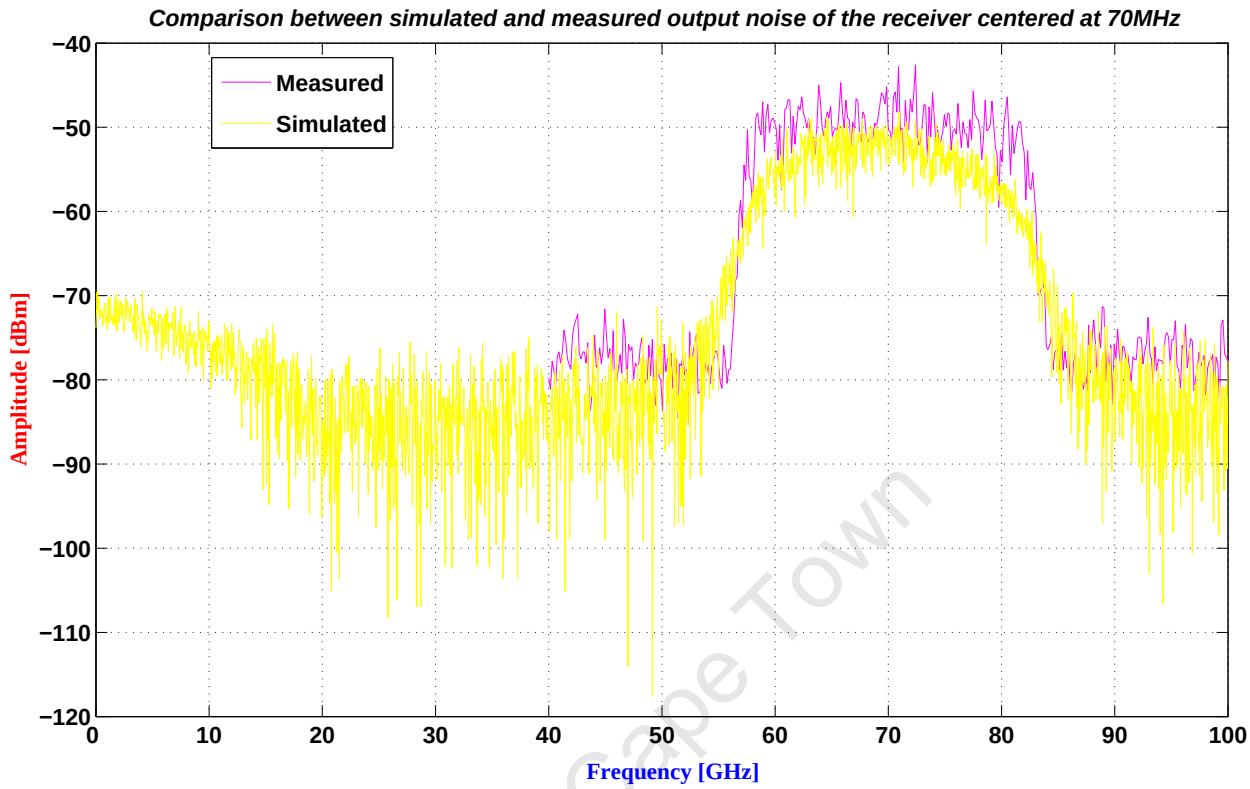

Figure 5.11: Receiver noise of the 24-Channel RF receiver at 70 MHz with a bandwidth of 24 MHz. The resolution and video bandwidth of the spectrum analyser used for conducting this test was set to 100 kHz respectively, with the simulation resolution bandwdith of 50 kHz.

Synthesiser 1		
Start Frequency (MHz)	Stop Frequency (MHz)	Product
3236	3248	3*LO1 - 4*LO2
3578	3594	3*LO2 - 2*LO1
3649	3664	3*LO2 - 2*LO1

Table 5.5: Spurious Signals found at the output of the RF receiver. For LO1 stands for synthesiser board 1 with a varying frequency from 3184 MHz to 4234 MHz and LO2 stands for synthesiser board 2 with a fixed oscillator frequency of 2554/2414 MHz. This is caused by the internal spurious signal of the second synthesiser board with the RF rack. The spur signal can be elimiated if the oscillator frequency for the second synthesiser board is set to 2454 MHz instead of 2414 MHz.

load resistor into liquid nitrogen and used it as the cold source. More information on the Y-factor test can be found in [27].

The laborary where the tests were conducted is not a RFI free environment and resulting different kinds of radiation around the area affects the accuracy of the tests. As discussed in Figure 5.6, it has shown that a 590 MHz unexpected spurious signal occurs in the measurement. Therefore it is crucial to perform tests in a RFI free environment or in a shielded room, if possible, to perform the tests to increase accuracy of the measurements.

5.1.9 Conclusion

This chapter discussed the acceptance test procedures and the results obtained from the measurements. Comparison between simulated and measured results were analysed and discussed. From the channel isolation test, it is found that the measured channel gain for each of the twenty-four channel at various RF input frequencies (700 to 1700 MHz) with an input power level of -50 dBm is lower than the simulated channel gain. One of the possible reason is that, the simulated results did not take into account the possible losses on the IF signals caused by the physical integration of the RF receiver rack. By comparing the measured and simulated dynamic range results of the 3x4 receiver module, it is shown that the simulated IF output power level is about 4 dBm less than the measured value, when an RF input power level at -70 dBm is injected into the RF receiver. Whereas the measured IF output power level with an input RF power of -34 dBm is about 4 dBm higher than the simulated result. From the channel intermodulation distortion test, it is found that an unwanted signal at 580 MHz was found. It is concluded that this is an interference TV signal received by the sensitive 24-channel RF receiver, and is unavoidable unless the test is performed in a interference free environment. By comparing the measured and simulated results for the receiver noise test, it is found that the noise floor of the receiver obtained from the simulation is 20 dB lower than that of the measured. This discrepancy is caused by the instrument noise floor of the spectrum analyser, and this could not be predicted using SystemView. From the channel gain control test, it is shown that the 6-bit programmable attenuator for each 3x4 receiver module is able to vary each its attenuation between 2 to 31 dB in 1 dB step via an external computer. The channel frequency response shows that the measured receiver noise is 10 dB higher than the simulated receiver noise due to the fact that the 24-channel RF receiver rack generates more noise than the predicted. In order to avoid spurious signals that were caused by the intermodulation products between the two synthesiser boards, the LO2 frequency is set to 2554 MHz instead of 2414 MHz. In the following chapter, conclusions and recommendation for this dissertation will be presented.

Chapter 6

Conclusion and Recommendation

In this dissertation, a general overview of how the KAT project led to this research was given. The fundamental design principles of the 3x4 receiver module including its achitecture and choice of components were discussed in Chapter 2. In addition, different receiver design parameters were investigated in this chapter in terms of theoretical analysis and mathematical calculations. It is found that the 3x4 receiver module has a linear dynamic range of 105 dB and a system gain varies from 39 to 68 dB. These parameters were used in the simulations in Chapter 3.

In Chapter 3, simulations of the 3x4 receiver module in SystemView were implemented to ensure that the xNDT receiver prototype from the Australian design was suitable for testing the two 3x4 Vivaldi antennas. It also described how the 3x4 receiver was simulated in the SystemView environment. Each of the components used in the 3x4 receiver was modelled in SystemView according to the specifications provided by the manufacturers. The simulation results were discussed, and it is concluded that the input RF power level must be within the specified operating range (i.e. -64 to -34 dBm). Otherwise, saturations of the receiver and intermodulation products would be generated. In addition, the power tracking simulation at each component output of the 3x4 receiver module in SystemView ensured that, the input power levels going into the components (especially amplifiers and mixers) did not exceed the specified power level, and hence saturate the components, resulting intermodulation products. From the two-tone test simulation result, it predicted correctly where the intermodulations would appear compared to the theoretical predictions.

In Chapter 4, a considerable effort was spent on understanding the integration of the 24-channel RF receiver rack by Tellumat (Pty) Ltd. Problems encountered during the integration were reviewed in this chapter. It has shown that all the sub-components were successfully integrated into the 19” rack.

In Chapter 5, acceptance tests procedures and laboratory test setup were discussed and results comparison between the simulated and measured data were analysed. By comparing the measured and simulation results, it is concluded that the Australian designed 3x4 receiver module is suitable to be used in the integration of the 24-channel RF receiver.

It was shown from the acceptance test results that the 24-channel RF rack integrated by Tellumat (Pty) Ltd has met the design specifications. and that SystemView do predict the behaviour of the 3x4 receiver correctly in high system level. But it is found that SystemView is adequate for simulating systems in system level only (for telecommunication systems or wireless logical systems). In terms of low level simulations such as IP3 points and noise figure, it was not possible to be simulated in SystemView. Therefore it is recommended that other simulation package such as Advanced Design System (ADS) by Agilent should be considered for more advanced receiver simulations. In this chapter, observation was found from the acceptance test that, the IFLO must set to 2554 MHz instead of 2414 MHz to avoid the occurrence of spurious signals generated by the local oscillators within the 24-channel RF rack. This phenomena was not being predicted in SystemView simulations, but was only observed after the 24-channel RF rack is being integrated by Tellumat (Pty) Ltd. Lastly, recommendation is suggested that the measurement results obtained in this research can be improved, if all the testing equipments were correctly calibrated. Another suggestion is to conduct the acceptance tests in the screened room (a room with RF spurious signals free environment). This will reduce the measurements error during the tests.

To conclude, the design and architecture of the 3x4 receiver module were studied in this research by conducting both theoretical analysis and simulations using SystemView. The testings performed on the 3x4 RF receiver rack were presented and measurements obtained were used to compare with the simulation results. It is understood that the 3x4 receiver module has met the specification to be integrated into the RF receiver rack, and that the fully integrated RF receiver rack by the contractor has met the user requirements.

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Appendix A

Contractor ATPs

A.1 Power Supply Unit

The Power Supply Unit (PSU) was tested to ensure that when the it is under full load, the DC output of the PSU would meet the voltages as specified on the manufacturer datasheet (i.e. +5 V, ±5 V and + 25 V) and hence provide the required power supply voltages to the RF rack. The laboratory setup for this test is illustrated in Figure A.1. In the figure, a DC voltmeter is connected to the output of the PSU to measure the DC output voltages. Table A.1 lists the predicted and measured DC output voltages of the PSU obtained under the full load test. Thereafter, ripple measurement at + 5 V and ±15 V under full load were conducted by connecting the oscilloscope to the DC output voltages of the PSU. The ripple measurements a +5 V and ±15 V under full load are shown in table A.1. It is proven from [2] that lower the ripple figure, the smaller the voltage ripple and hence better performance of the PSU. It can be concluded that the PSU under test has met the specified voltages requirement and is capable of providing the required voltages to the 24-channel RF receiver.

A.2 Local Oscillators' Frequency and Power

The objectives for testing the local oscillators are listed below:

- To measure, by connecting the spectrum analyser to LO1 and LO2 Synthesiser boards respectively, the local oscillator frequencies can be tuned as required in the specification.
- To measure, by connecting the spectrum analyser to LO1 and LO2 Synthesiser boards respectively, the output power level before and after the splitter network.
- To measure, by connecting the network analyser to LO1 and LO2 Synthesiser boards respectively, the phase and amplitude imbalance between all the twenty-four ports after the splitter network.

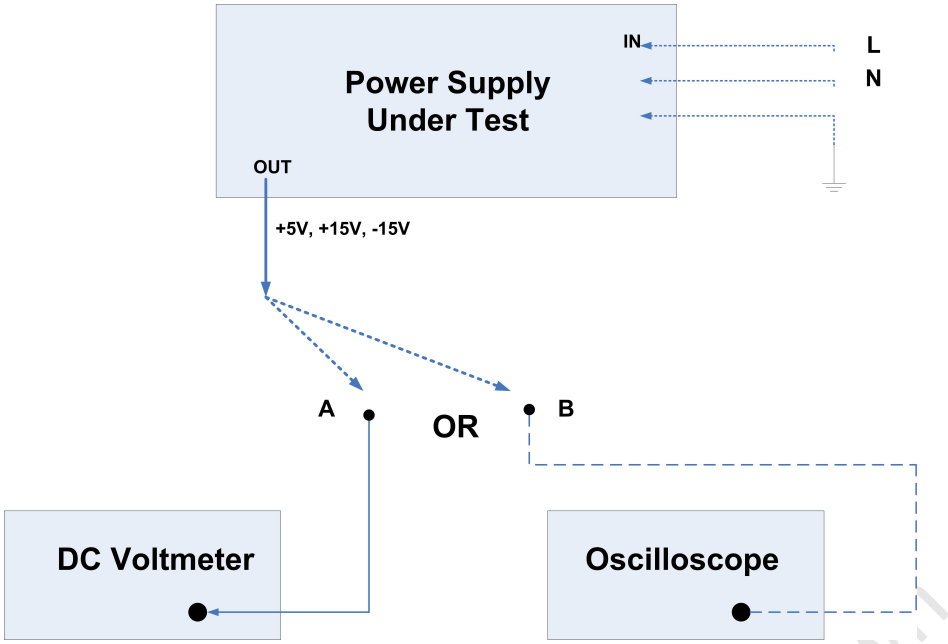

Figure A.1: Power supply unit (PSU) test measurement setup. The output of the PSU is connected to the DC voltmeter (refer to A in the figure) for measuring the DC output voltages. For ripple measurements, an oscilloscope (refer to B in the figure) is connected to the output of the PSU instead.

	Expected Voltage - Vexpected (V)	Measured Voltage - Vmeasured (V)	Measured Ripple- Vripple (V)	Voltage Ripple in (%)
Voltage measured at +5V pin under full load	+5V	+5.65V	0.36V	7.2
Voltage measured at +15V pin under full load	+15V	+15.02V	0.64V	4.3
Voltage measured at -15V pin under full load	-15V	-14.99V	0.4V	0.4
Voltage measured at +25V pin under full load	+25V	+24.08V	-	-

Table A.1: Expected and measured voltages obtained from the PSU full load test.

The laboratory setup for testing the amplitude and phase imbalance between ports for LO1 synthesiser is shown in Figure A.2. As shown in the figure, the input of the splitter is connected to port S1 of the network anlyser 8753D, and with the output of the splitter connected to the S2 port of the same network analyser. The S21 (transmission coefficient) is measured between the common port (J4) and the rest of the twenty-three ports.

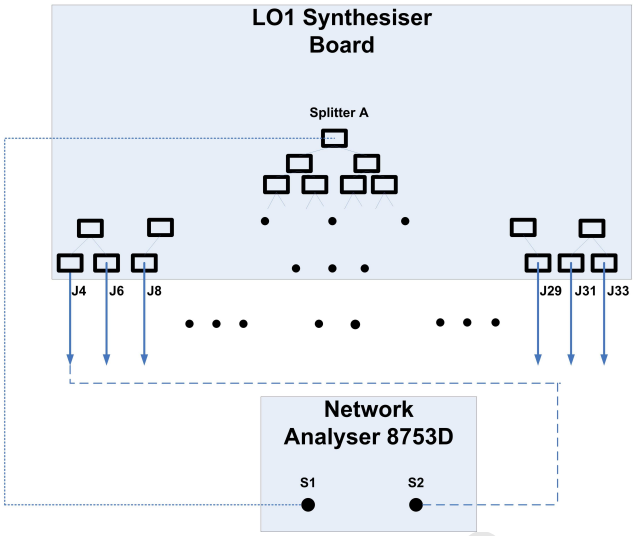

Figure A.2: Test setup for amplitude and phase imbalance between the twenty-four output ports of LO1 Synthesiser board is shown. The same test setup was used for LO2 Synthesiser board.

The common port J4 was chosen arbitrarily for measuring the amplitude and phase imbalance between the other twenty-three ports of LO1 Synthesiser board. The expected amplitude imbalance between any two ports of LO1 synthesiser board must be $\leq$1.5 dB, whereas the phase imbalance between any two ports must be $\leq$10 deg . As shown in Figure A.3, the amplitude of port J4 is compared with the amplitude of the other twenty-three ports in dBm. It indicates that the amplitude of the two ports (J8 and J11) have exceeded the power level by 0.5 dB as specified. But this can be regarded as a result of inaccurate measurements because the test was not conducted in a RFI free environment. In Figure A.4, the phase value of the ports lie within the specified range and it also shows that as the input frequency reaches its maximum frequency (i.e. 4200 MHz), the phases between ports fluctuate more. Therefore it is crucial to ensure that the amplitude and phase measured at the outputs of each port are within the specified range over the operating frequency range. This can avoid degradation in receiver performance if each LO output ports can provide stable output power level.

The output power level at the specified frequency (low, mid and high band) were recorded to ensure that the local oscillators have provided enough power to be distributed to the receiver modules at the programmed frequency. From the acceptance tests result, the performance of LO1 and LO2 synthesizer boards developed by Tellumat (Pty) Ltd can be concluded as follows:

- LO1 synthesiser board can be programmed at its tunable operating frequency range

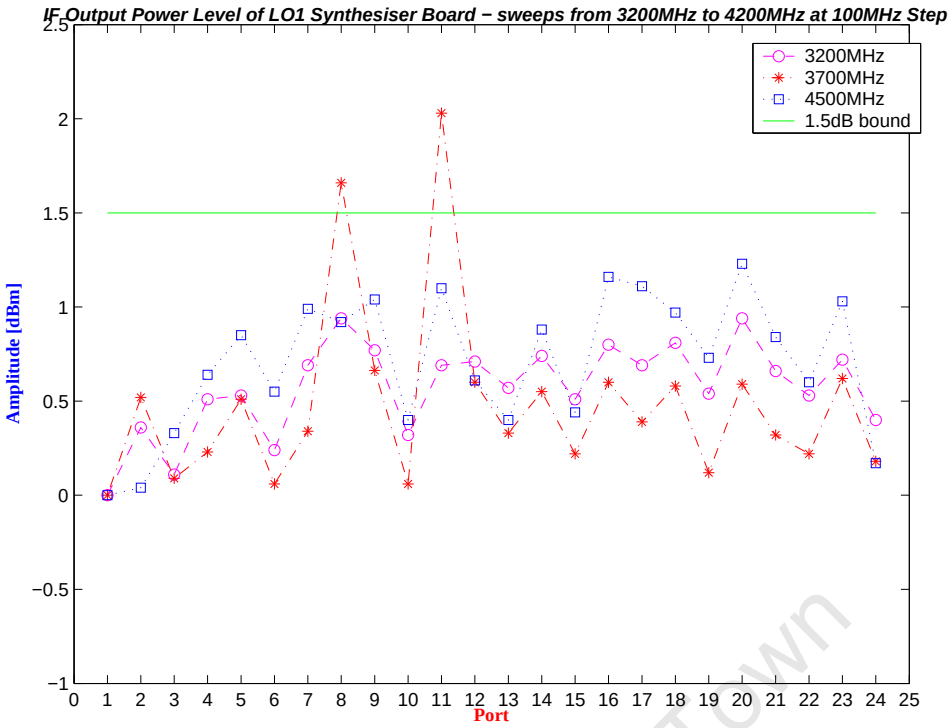

Figure A.3: Amplitude imbalance measurement for LO1 Synthesiser board are plotted. The amplitude of port J4 is compared with the rest of the twenty-three ports. The measurements were taken at low, mid and high operating frequency band of LO1 synthesiser board (3200MHz, 3700MHz, and 4200MHz). It is shown that two values have exceeded the required amplitude.

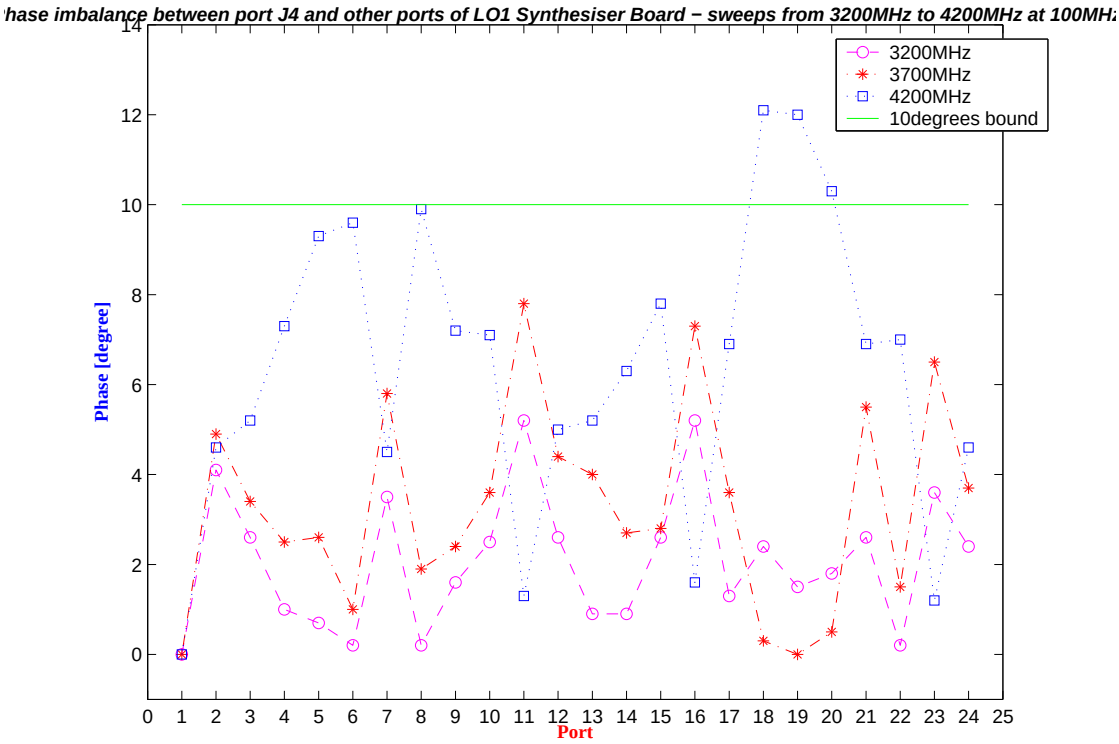

Figure A.4: Phase imbalance measurements for LO1 synthesiser board are plotted. Phase of port J4 was measured and compared with the other twenty-three ports of LO1 synthesiser board. Measurements were conducted at low, mid and high operating frequency (3200MHz, 2700MHz and 4500MHz).

in a step of 100 MHz (i.e. from 3200 MHz to 4200 MHz). LO2 synthesiser board can be programmed at its fixed operating frequency of 2414 MHz. (and also at 2454 MHz, which is the RF2 - IF)

- The amplitude imbalance between each output ports of the synthesiser boards lied within the specified range.
- The phase imbalance between each output ports of the synthesiser boards lied within the specified range. Except for LO1 synthesiser board, the phase tends to fluctuate more as the frequency increases, but it still lies within the specified error range.
- The power level of each output ports for LO1 and LO2 synthesisers are enough to drive the receiver modules on the motherboards.

A.3 Motherboards

The output voltages of the LO ports (namely, RFLO and IFLO) on the motherboards were measured using the power meter. The test setup is shown in Figure A.5. The output voltages supplied by the two local oscillators (LO1 and LO2) to the LO output ports on the motherboards were measured at 3.484 GHz for RFLO port and 2.414 GHz for IFLO port. The measurements were conducted when the 24-channel RF receiver rack was fully integrated but the receiver modules were not mounted on the motherboards. Figure A.6 and A.7 show the measurements obtained from the tests for the two motherboards at 3484 MHz and 2414 MHz for RFLO and IFLO port respectively. The average output voltages for IFLO port at 2414 MHz is 1.69 V and for RFLO port at 3484 MHz, an average output voltage of -0.41 V is achieved. These obtained results has met the specification requirement.

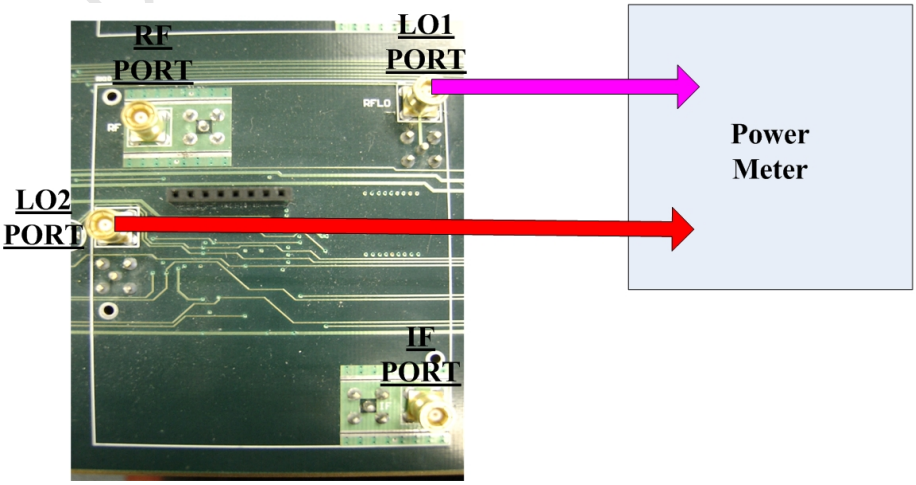

Figure A.5: The test setup for measuring the output voltages of RFLO and IFLO ports for one module of the motherboard is shown. The same test is repeated for all the modules on both of the motherboards.

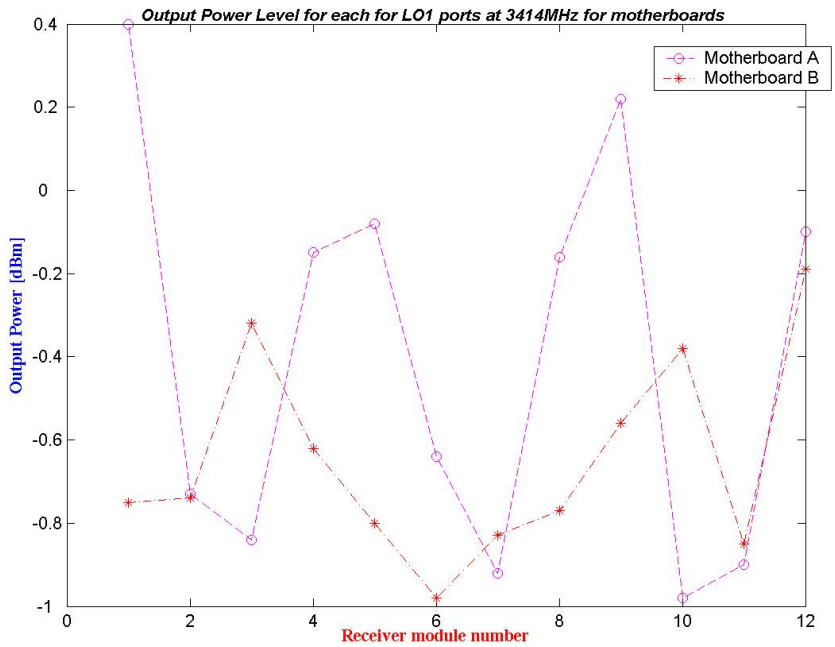

Figure A.6: The test setup for measuring the output voltages of RFLO and IFLO ports for one module of the motherboard is shown. The same test is repeated for all the modules on both of the motherboards.

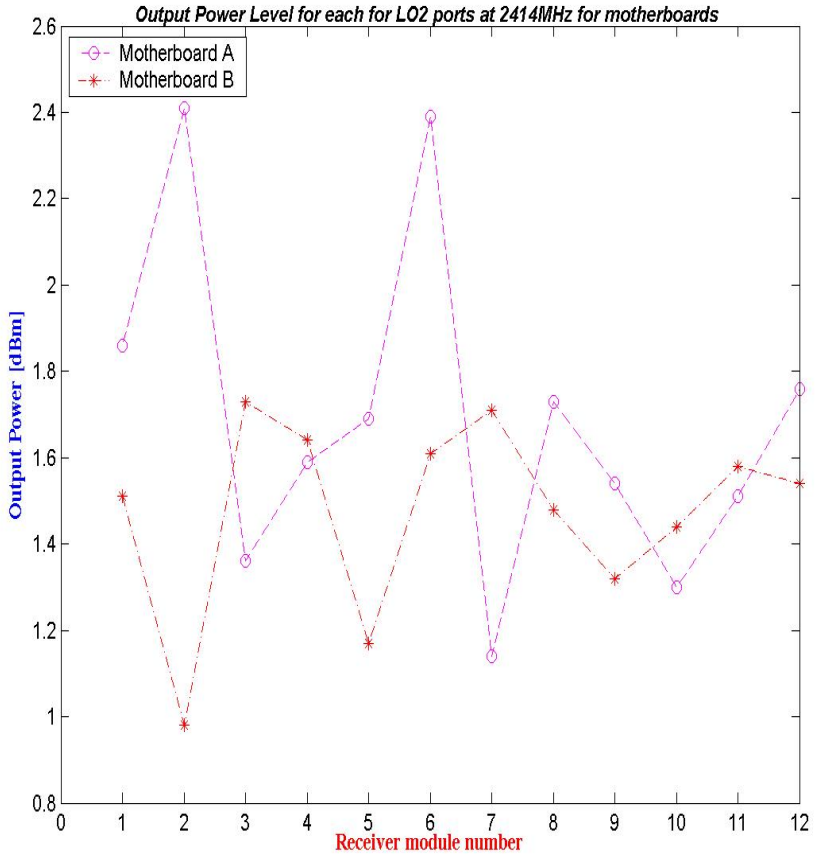

Figure A.7: Output voltages measured at each IFLO port at 2484 MHz on motherboard A. Output voltages were measured in the same way for motherboard B.

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